Abridged Common Management Interface Specifications (ACMIS)

Revision 0.95a

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REVISION HISTORY

Revision	*Date*	*Objective*	*By*
ACMIS Rev0.9a	*9/19/2018*	*Draft for review and comment*	*Jiashu Chen*
ACMIS Rev 0.93a	*10/11/2018*	*Draft for publish and review*	*Jiashu Chen*
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REFERENCES

1. Specification for Dual SMALL FORM FACTOR PLUGGABLE MODULE, Rev. 1.0, September 12, 2018
2. CMIS Rev. 3.0 (draft)
3. SFF-8636 Specification for Management Interface for Cabled Environments Rev 2.6
4. SFF QSFP28 MSA
5. OSFP MSA (Hardware Specification)
6. QSFP-DD MSA (Hardware Specification)
7. CFP MSA Management Interface Specification Version 2.6 (R06a)
8. 400G-FR4 Technical Specification Rev. 2.0

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1 DOCUMENT SUMMARY

1.1 Introduction

This document is an Abridged CMIS (ACMIS) for simplified support of DSFP, QSFP56, and OSFP modules. The main objective is to reduce the complexity of host and module software. ACMIS memory map is a subset of CMIS and will evolve with CMIS. ACMIS makes the following changes/additions.

1) A single module state machine is defined for managing the module startup process and operation.
2) module for simplicity. Multiple lane mapping advertisement has been simplified to a few registers from 60+ registers.
3) CMIS Data Path construct and associated state machines eliminated from the
4) Module configuration and start up process simplified with Module Control Register Set, Boot Record, and MBR Manager to set up applications of whole module at once.
5) Application Selection counts increased to 32 from 15. Each Application Selection only contains 2 bytes down from 6. Application Select has been simplified to writing 8 Per Lane Application Select registers.
6) Generalized Command-Data-Block added to handle complex processes for bulk data transfer with handshaking protocol between host and module.
7) PRBS support added.
8) Firmware upgrade function is supported.
9) Eye quality monitor function is proposed.
10) All rights are reserved to at any time to add, amend, or withdraw technical data contained in this document.

1.2 ACMIS Content

ACMIS consists of 6 chapters. Chapter 1 is the overview. Chapter 2 is about Two Wire Interface (TWI) which is direct copy of corresponding section from CMIS Rev.2.91. Chapter 3 describes the control and signal theory between a host and a module. Chapter 4 illustrates typical applications using the theory and memory map. Chapter 5 is register definition. An appendix is added as Chapter 6.

1.3 Notations

1.3.1 Number Notations

Hex numbers are post-fixed by a lower-case letter “h”, for example, FEh. Binary numbers are post-fixed by a lower-case letter “b” such as 11b and 1101b. Decimal numbers have neither prefix nor postfix.

1.3.2 Page, Byte, and Bit reference

TWI memory map consists of low memory and high memory. The high memory contains multiple pages. For examples, Bit 7 of Byte 25 in Lower Page shall be designated as

L0h.25.7 or 25.7 when context is clear. Bit 7 of byte 255 on Upper Page 02h shall be designated as U2h.128.7, or U2.128.7. When hex number or binary number is used the number notations in section 1.3.1 shall be used.

1.3.3 Glossary

The often-used nomenclatures in this document are listed in the following glossary table for reference.

Table 1 Glossary

Terminology	Description
Application Code	Any of a set of specific codes of 13 bits as defined in SFF-8089's ACT. When written into the AST, 3 additional bits are appended to the Application Code to define HW control.
Application Code table	Table in 8089 that defines numerous standardized Application Codes from which a module vendor can choose fro writing into the module's AST.
ApplicationSelect	An extended version of RateSelect, defined in SFF-8079 Part 2, ApplicationSelect is backward compatible with Extended RateSelect and RateSelect.
CDR	Clock and data recovery.
CLEI	Common Language Equipment Identification, a 10-byte field that contains vendor's CLEI code in ASCII characters.
Control	It refers to the Host control functions to the module over Management Interface. It also includes the support of control pin logic.
Custom	Custom fields and formats are defined by the module vendor and may be unique to a specific vendor.
DFB	Distributed Feedback laser.
DDM	Digital Diagnostic Monitoring. It includes Module functions of A/D value reporting, FAWS logic, and programmable alarm pin logic.
Exteneded RateSelect	An extended version of RateSelect, defined in SFF-079 Part 1, for specific anticipated multi-rate module requirements. RateSelect and Extended RateSelect logically OR the control from rate_select and Extended RateSelect logically OR the control from rate_select and soft_rate_select, if both inputs are used.
FAWS	The short-hand abbreviation for Fault, Alarm, Warning, and Status, term was first time introduced in CFP MSA MIS.
MBR	Module Boot Record – a data structure introduced in ACMIS Rev. 0.94b for storing all the initial values of VRs determining the power on behavior of a module.
NVM	Non-Volatile Memory.
NVR	Non-Volatile Register.
OM2	Cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 1500 MHz-km at 850 nm as IEC 607093-10 Type A1a.1 fiber.
OM3	Cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 1500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 2000 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.2 fiber.
OM4	Cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm in accordance with IEC 60793-2-10 Type A1a.3 fiber.
OM5	Cabled optical fiber containing 50/125 um laser optimized multimode fiber with a minimum overfilled launch bandwidth of 3500 MHz-km at 850 nm, 1850 MHz-km at 953 nm and 500 MHz-km at 1300 nm as well as an effective laser launch bandwidth of 4700 MHz-km at 850 nm and 2470 MHz-km at 953 nm in accordance with IEC 60793-2-10 Type A1a.4 fiber.
OMA	Optical Modulation Amplitude - The difference between two optical power levels, of a digital signal generated by an optical source, *e.g.,* a laser diode.
PAM4	Pulse Amplitude Modulation, four levels (PAM4), a modulation scheme where two bits are mapped into four signal amplitude levels to enable transmission of two bits per symbol.
PMD	Physical Medium Dependent.

Terminology	Description
RateSelect	The original function of controlling a module, typically receiver bandwidth, as defined in INF-8074 (via rate_select) and enhanced in SFF-8472 (via soft_rate_select).
User	The customer of Module.
Vendor	The manufacturer of Module.

1.4 ACMIS Publication and Revision Process

This document is maintained by its editing and project management team. It starts as a draft and hosted by DSFP website. Once it becomes formal publication, updates to this document shall be drafted, reviewed, and published in the form of addendums to a specific revision of this document. These addendums shall be integrated into next revision of ACMIS and this cycle repeats during the life cycle of it.

2 TWO WIRE INTERFACE (TWI) MANAGEMENT INTERFACE

2.1 Introduction

Communication between Host and Module is done via a Two Wire serial Interface(TWI). Detailed electrical specifications and TWI timing are given in the appropriate hardware/module specification.

2.2 Management Interface Timing Specification

The management interface timing requirements are defined in the appropriate hardware specification. The TWI address of the module is 1010000X (A0h). The host shall initially address the module using a 0-400KHz SCL clock speed. If a higher management interface speed is supported, the host may switch the 0-1MHz SCL clock speed.

In order to allow access to multiple modules on common TWI bus, some form factors support module select signal, (ModSelL). ACMIS does not support ModSelL. Instead each module requires a dedicated TWI bus. This is also a requirement for higher clock speed TWI bus operation.

2.3 Signal Interface

The TWI shall consist of a master and slave. The host shall be the master and the module shall be the slave. Control and data are transferred serially. The master shall initiate all data transfers. Data can be transferred from the master to the slave and from the slave to the master. The TWI shall consist of clock (SCL) and data (SDA) signals.
The master utilizes SCL to clock data and control information on the TWI bus. The master and slave shall latch the state of SDA on the positive transitioning edge of SCL.
The SDA signal is bi-directional. During data transfer, the SDA signal shall transition when SCL is low. A transition on the SDA signal while SCL is high shall indicate a stop or start condition.

2.4 Serial Interface Protocol

2.4.1 Operational States and State Transition

2.4.1.1 Start

A high-to-low transition of SDA with SCL high is a START condition. All TWI bus operations shall begin with a START condition.

2.4.1.2 Stop

A low-to-high transition of SDA with SCL high is a STOP condition. All TWI bus operations shall end with a STOP condition

2.4.1.3 Acknowledge

After sending each 8-bit word, the side driving the TWI bus releases the SDA line for one bit time, during which the monitoring side of the TWI bus is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Write data operations shall be

acknowledged by the slave for all bytes. Read data operations shall be acknowledged by the master for all but the final byte read, for which the master shall respond with a non-acknowledge (NACK) by permitting SDA to remain high and followed by a STOP.

2.4.1.4 Clock Stretching

To extend the transfer the slave asserts clock low. This should be initiated while the clock is low. This can be used by the slave to delay completion of the operation.

2.4.2 Reset TWI

2.4.2.1 Power On Reset

The interface shall enter a reset state upon Application of power.

2.4.2.2 TWI Protocol Reset

Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

a) The master shall provide up to nine SCL clock cycle (drive low, then high) to the slave
b) The master shall monitor SDA while SCL is high on each cycle.
c) If the slave releases SDA, it will be high and the master is then free to initiate a START operation for the next transaction
d) If SDA remains low after a full nine clock cycles the TWI protocol reset has failed

2.4.2.3 Reset Signal

Some implementations may include a reset signal. If provided, upon assertion of the reset signal the TWI shall transition to the reset state.

2.4.3 Format

2.4.3.1 Read/Write Controls

After the start condition, the first 8-bit word of a TWI bus operation shall consist of '1010000' followed by a read/write control bit.
The least significant bit indicates if the operation is a data read or write. A read operation is performed if this bit is high and a write operation is executed if this bit is set low. Upon completion of the control word transmission the slave shall assert the SDA signal low to acknowledge delivery (ACK) of the control/address word.

2.4.3.2 Address and Data

Following the read/write control bit, addresses and data words are transmitted in 8-bit words. Data is transferred with the most significant bit (MSB) first. Multiple Byte transactions shall be transmitted in increasing byte address order over the TWI.

2.5 Read/Write Operations

2.5.1 Slave Memory Address Counter (Read and Write Operations)

All TWI slaves maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the slave. This address remains valid between operations as long as power to the slave is maintained. Upon loss of power to or reset of the module or upon transactions not terminated by a Stop condition, the slave address counter contents may be indeterminate. The address roll-over during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page. The host shall use single 2-byte reads to retrieve all 16-bit data, to guarantee data coherency. The module shall prevent the host from acquiring partially updated multi-byte data during a 2-byte read. Clock stretching provides one mechanism to delay the delivery of data until all bytes of one field have been updated.

2.5.2 Read Operations

2.5.2.1 Current Address Read

A current address read operation requires only the slave address read word (10100001) be sent. Once acknowledged by the slave, the current address data word is serially clocked out. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

Figure 1 Module Current Address Read Operation

		← CONTROL WORD →																		
MASTER	START	MSB						LSB	READ										NACK	Stop
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
SLAVE										ACK	MSB							LSB		
		<---- DATA WORD ----->																		

2.5.2.2 Random Read

A random read operation requires a dummy write operation to load in the target byte address. This is accomplished by the following sequence: The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the slave. The master then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The slave acknowledges the device address and serially clocks out

the requested data word. The transfer is terminated when the master responds with a NACK and a STOP instead of an acknowledge.

Figure 2 Module Random Read

		<--CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL WORD -->																		
START	MSB						LSB	READ										NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
									ACK	MSB							LSB		
										<---- DATA WORD n---->									

2.5.3 Sequential Read

Sequential reads are initiated by either a current address read (see Figure 3 Sequential Address Read Starting at Module Current Address) or a random address read (see Figure 4 Sequential Address Read Starting with Random Module Read). To specify a sequential read, the host responds with an acknowledge (instead of a STOP) after each data word. As long as the module receives an acknowledge, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledge.

Figure 3 Sequential Address Read Starting at Module Current Address

		<- CONTROL WORD -->																
MASTER	START	MSB						LSB	READ									ACK
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK	MSB							LSB	
											<---- DATA WORD n---->								

1

									ACK										NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1			
MSB							LSB		MSB							LSB				
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->											

2 **2.5.3.1 Sequential Read from Random Start Address**

3 Bit patterns of sequential read from random start address is depicted in Figure 4 Sequential
4 Address Read Starting with Random Module Read.

5 **2.5.4 Write Operations**

6 A write operation requires an 8-bit data word address following the device address write
7 word (10100000) and acknowledgement. Upon receipt of this address, the slave shall again
8 respond with a zero (ACK) to acknowledge and then clock in the first 8-bit data word.
9 Following the receipt of the 8-bit data word, the slave shall output a zero (ACK) and the
10 master must terminate the write sequence with a STOP condition for the write cycle to
11 begin. If a START condition is sent in place of a STOP condition (i.e. a repeated START
12 per the TWI specification) the write is aborted and the data received during that operation is
13 discarded. Upon receipt of the proper STOP condition, the slave enters an internally timed
14 write cycle, tWR, to internal memory. (See appropriate Hardware specification for tWR
15 timing) The slave disables its management interface input during this write cycle and shall
16 not respond or acknowledge subsequent commands until the internal memory write is
17 complete. Note that TWI 'Combined Format' using repeated START conditions is not
18 supported on write commands.

Figure 4 Sequential Address Read Starting with Random Module Read

		<- CONTROL WORD -->									<BYTE OFFSET ADDRESS>								
MASTER	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
SLAVE										ACK									ACK

	<- CONTROL WORD -->																	
START	MSB						LSB	READ										ACK
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	0
									ACK	MSB							LSB	
										<---- DATA WORD n---->								

								ACK									NACK	STOP
x	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x	1	
MSB							LSB		MSB							LSB		
<-- DATA WORD n+1 --->									<-- DATA WORD n+x --->									

Figure 5 Module Byte Write Operation

		<- CONTROL WORD ->									<BYTE OFFSET ADDRESS>									<- DATA WORD ->									
MASTER	START	MSB						LSB	WRITE		MSB							LSB		MSB							LSB		STOP
		1	0	1	0	0	0	0	0	0	x	x	x	X	x	x	x	x	0	x	x	x	x	x	x	x	x	0	
SLAVE										ACK									ACK									ACK	

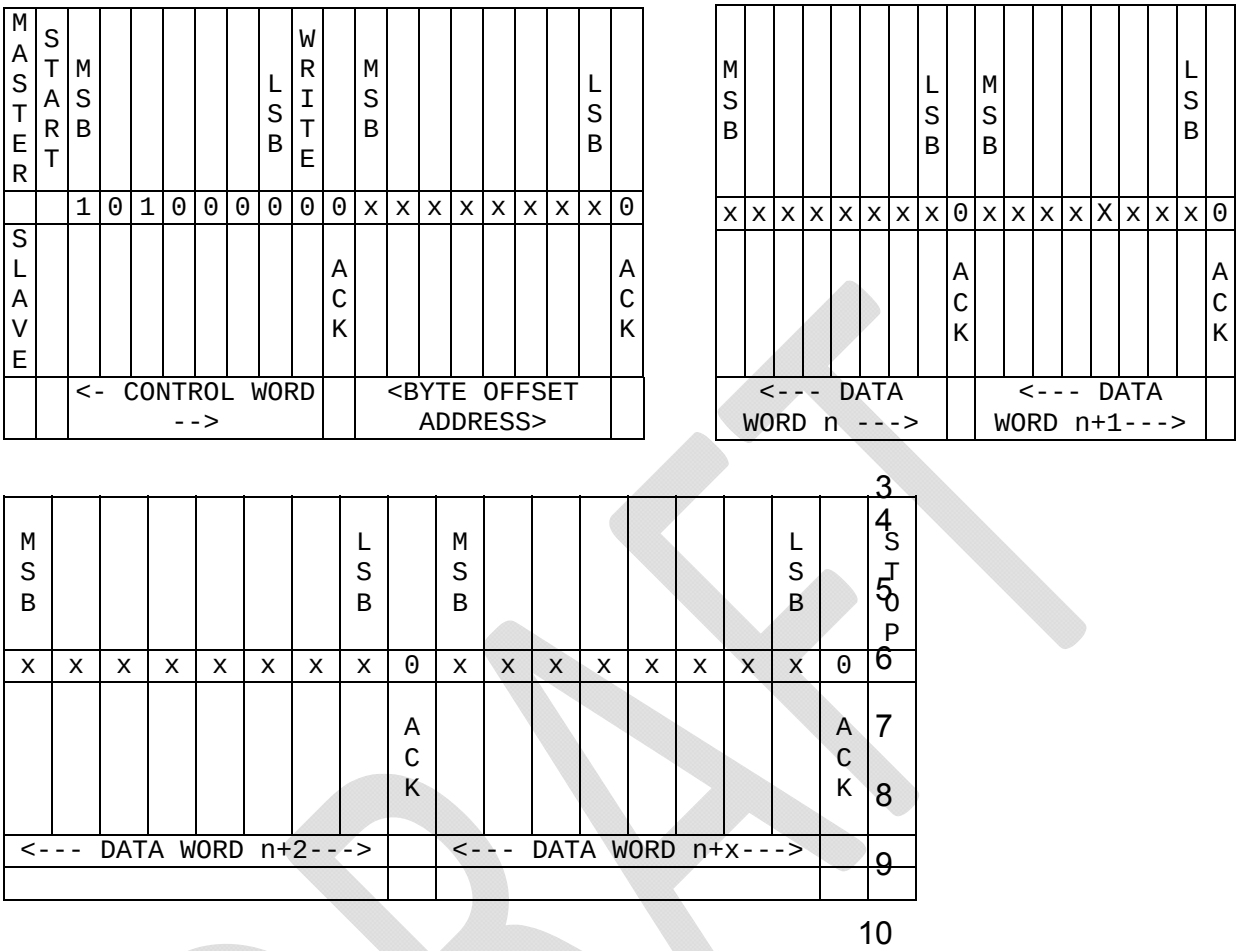
2.5.4.1 Sequential Write

The TWI slave shall support a sequential byte write to non-volatile memory of up to eight bytes without repeatedly sending slave address and memory address information. The number of sequential writes to volatile memory is not limited. In a sequential write, the host should not include in the sequence a mixture of volatile and non-volatile registers. It should be noted that at the end of each 128 byte page, the next address rolls over to the first byte of the same page.

A sequential write is initiated the same way as a single byte write, but the host master does not send a stop condition after the first word is clocked in. Instead, after the slave acknowledges receipt of the first data word, the master can transmit additional data words: seven additional words for non-volatile memory and unlimited for volatile memory. The slave shall send an acknowledge after each data word received. The slave may act on write data after generating the acknowledge and may buffer the write transaction.
The master must terminate the sequential write sequence with a STOP condition. Upon receipt of the proper Stop condition, for writes to non-volatile memory, the slave may enter an internally timed write cycle, tWR, to internal memory. The slave disables its management interface input during this write cycle and shall not respond or acknowledge subsequent commands until the internal memory write is complete. If there is no proper STOP condition, the results of the sequential write are unpredictable.

Note that TWI 'combined format' using repeated START conditions is not supported on write commands.

Figure 6 Module Sequential Write Operation



2.5.4.2 Acknowledge Polling

Once the module internally timed write cycle has begun (and inputs are being ignored on the bus) acknowledge polling can be used to determine when the write operation is complete. This involves sending a START condition followed by the device address word. Only if the internal write cycle is complete shall the module respond with an acknowledge to subsequent commands, indicating read or write operations can continue.

2.6 Timing for Soft Control and Status Functions

Timing for module soft control, status functions, and squelch and disable timings can be found in the appropriate Module Hardware Specification.

3 MODULE MANAGEMENT

In this chapter, ACMIS specifies the basic operations of a transceiver module with the following topics.

- Module basic structure
- Module state machine
- Application Selection
- Module configuration and startup sequence

3.1 General Module Architecture

A module consists of a transmitter (TX) and a receiver (RX) that exchange high speed data between host and media network, either electrically or optically. Each TX or RX has one or more parallel lanes for higher data throughput. The Host and Media may process data at different rate and hence the host lanes and media lane may have different lane count and different data rate, involving different multiplexing schemes. Figure 7 Module Block Diagram depicts the block diagram of a module.

3.1.1 Host Lane

A host lane is the host interface of a module and may contain CDR, gearbox, equalizer, and other devices for host side signal conditioning. These devices can be lane proprietary or shared among multiple host lanes.

3.1.2 Media Lane

A media lane is the network interface of a module and may contain media dependent driver, TIA, equalizer, and other signal conditioning devices. These devices can be lane proprietary or shared among multiple media lanes, depending upon implementation.

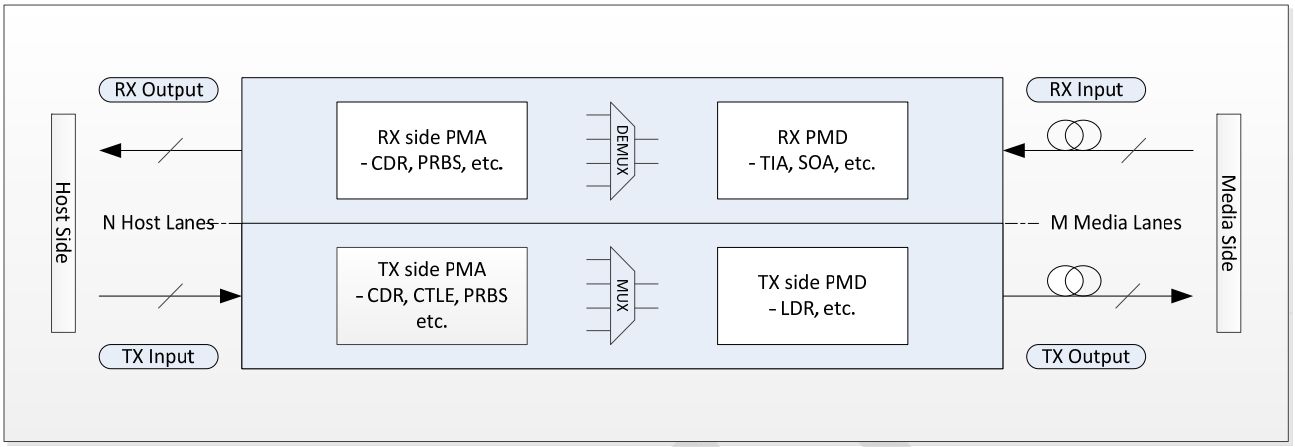
3.1.3 Mux and De-mux (SERDES)

Multiplexer (MUX) and demultiplexer (additional electronics as well) are commonly used to convert the data rate and signal format. The use of MUX and DeMUX results in different host and media lane counts.

3.1.4 Management Interface

While not showing in the block diagram, module has a management interface, usually consists of a number of hardware pins (pads) and a two-wire interface (TWI). Hardware pins perform typically are used for host to control the module and for module to report critical conditions to host in, a timely manner. The TWI runs a serial communication protocol to allow host to read and write to module's memory map.

Figure 7 Module Block Diagram



3.1.5 Resource Management

A module may have resources, such as lasers, modulators, microcontrollers, mux/demux IC's. These resources shall be managed at difference level of control by host and module, depending upon module state (see below Module State Machine) and module configuration (see section 3.5). The following sections describe these resources and their general ownership. The behavior of control on these resources are specified in Table 5 Module and Lane Behavior per State.

3.1.5.1 Module Common Resource

In most of the cases the module contains resources common to partial or all data lanes. These resources may include TWI, management interface pins, MCU and firmware, digital logic, power supplies, TECs, and others. These resources shall be fully powered or partially powered depending upon module states and power up sequence.

3.1.5.2 Lane Shared Resources

Depending upon implementation, lanes may be grouped together in sharing common resource such as TEC or MUX/DEMUX. A typical example is for 8 media lanes, every 4 lanes can share one TEC. In this case TEC may need to be powered up even there is only one lane active.

3.1.5.3 Lane Individual Resources

Depending upon implementation, each lane may have its individually owned resources such as CDR or Laser driver. These resources can be individually controlled even multiple instances are implemented on a monolithic IC or other device format.

3.1.6 Lane Designations

Based on Figure 7 Module Block Diagram the following terms are established and are referenced in this document.

RX host lane, RX media lane, RX Output, RX input, and
TX host lane, TX media lane, TX input, TX output.

3.1.7 Lane Banking

In addition to Page Select Byte at address 127 (7Fh), the Bank Select Byte is added at address 126 (7Eh). When Bank Select = 0, lanes 1~8 are addressable. When Bank Select = 1, lanes 9 to 16 are addressable, and so on so forth. It is noted that higher bank lanes repeat the full characteristics of Bank 0 lanes. In the current version of ACMIS, banking applies to upper pages 10h~1Fh to support more than 8 lanes.

3.2 Module State Machine

To facilitate a well-defined module startup and module turn-off sequences and other applications, ACMIS specifies a list of module states that a module shall support.

Note passive cable does not need to support module state machine.

In association with these states, a set of signals that are related to state transitions are also defined. In the following text, a signal name with a lower-case "s" suffix stands for a combination of multiple signals.

3.2.1 Hardware Control and Signaling Pins

Table 2 Module Hardware Pin and Alias presents an overview of hardware pins and their equivalence among several form factors. Based on the description provided, the following observations/assumptions are made,

1) All form factors have 4 common hardware pins, Module Reset, Module Low Power Mode, Module Present, and Host Interrupt.
2) QSFP-DD InitMode pin is treated as LPMode pin, i.e. the same as for QSFP28 and QSFP56.
3) Module Present function is the same across all form factors
4) The Module Select pin of QSFP form factors is not the focus and it is assumed each module to have a dedicated TWI bus.
5) Module Reset and Module Low Power Mode pins are module inputs from host.
6) Module Present and Host Interrupt pins are module outputs to host.

Table 2 Module Hardware Pin and Alias

HW I/O PIN LOGIC ALIAS*	QSFP28 & QSFP56	DSFP & OSFP	QSFP-DD
Module_Select_Pin	ModSelL**	N.A.	ModselL**
Module_Reset_Pin	ResetL	RSTn	ResetL
Module_Low_Power_Pin	LPMode	**NOT** LPWn	InitMode***
Module_Present_Pin	ModPrsL	PRSn	ModPrsL
Module_Interrupt_Pin	**NOT** IntL	INT	**NOT** IntL
Two Wire Interface (TWI) pins	SDA/SCL	SDA/SCL	SDA/SCL
*All aliases represent active high logic in CMOS. 1 = physical pin logic asserted, 0 = physical pin logic de-asserted cross form factors. **ModSelL is not supported and is ignored by ACMIS. *** QSFP-DD InitMode pin is treated same as QSFP28 or QSFP56 LPMode pin.			

3.2.2 TWI Register Bits equivalent to Hardware Pins

ACMIS specifies functionally equivalent TWI register bits for above mentioned hardware pins across different form factors in Table 3 TWI Register Bits Equivalent to Hardware Pins.

Table 3 TWI Register Bits Equivalent to Hardware Pins

TWI SIGNAL BIT LOGIC ALIAS**	QSFP28 & QSFP56	DSFP & OSFP	QSFP-DD
Module_Select_Bit	None	None	None
Module_Reset_Bit	None	Software Reset (26.3) *	Software Reset (26.3) *
Module_Low_Power_Bit		ForceLowPwr (26.3) *	ForceLowPwr (26.3) *
Module_Present_Bit	None	None	None
Module_Interrupt_Bit		Interrupt (3.0) *	Interrupt (3.0)*
*All aliases use active high logic. 1 = bit logically asserted, 0 = bit logically de-asserted cross form factors. ** (26.3) = Byte 26 bit 3 in low memory space, similarly (3.0) = Byte 3 bit 0, and so on. For register bit in high memory space a format of x.y.z is used, where x is the page number, y is the byte address, and z is the bit number.			

3.2.3 Module Internally Generated Logic Signals

This ACMIS specifies the following internally generated logic signals that affect module state transition and operation. Note these signals are defined by aliases defined in Table 4 Module Internally Generated Logic Signals.

Table 4 Module Internally Generated Logic Signals

LOGIC SIGNAL NAME	DEFINITION
ResetS	Module_Reset_Pin **OR** Module_Reset_Bit **OR** Vcc_Reset*
LowPwrS	(LPMode AND NOT LPModeOverride) OR ForceLowPwr
FaultS	Logic **OR** of all fault condition bits in Fault register.
*Vcc_Reset is an internally generated logic signal indicating Vcc does not meet vendor specified range, which may cause circuit malfunction or MCU brown-out.	

3.2.4 Module State Machine

Figure 8 Module State Transition Diagram**Error! Reference source not found.** depicts the 4 steady states and 4 transient states, as well as the conditions for this state machine transitioning from one to the next.

Host shall read register U00h.3 to determine the current state and to expect the module behavior according to Table 5 Module and Lane Behavior per State. Host shall determine the validity of alarms and warnings listed in Table 7 Module and Lane Flag Compliance to State.

The general utility of module state machine is to guide host through the module power up/down process during which time, the module behaviors change. With the definition of each state, module behavior is defined. Hence host can effectively manage the power up/down process instead of depending upon a time elapsing (waiting for 300 ms, e.g.). A

typical example of such utility is a false alarm of TX power low when module is in low power mode. Host is distracted to handle the interrupt due to this false alarm.

3.2.4.1 Steady State and Transient States

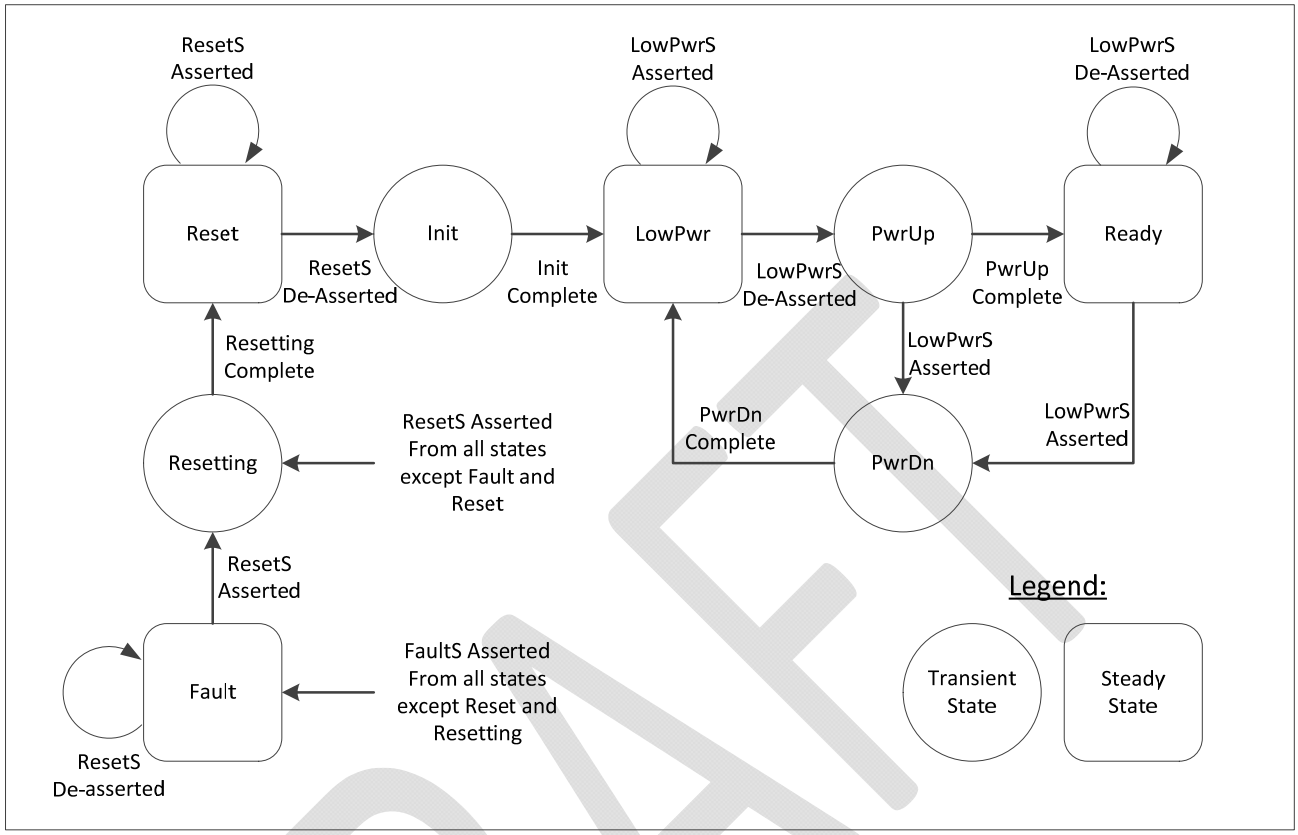
A steady state in module state machine maintains an iterative process when the behaviors of the state maintain unvaried until the input signals change. ACMIS specifies 4 steady states, Reset state, LowPwr(low power) state, Ready state, and Fault state.

A transient state in a module state machine represents a process when the behaviors of the state change over the time and eventually exits to another state. ACMIS specifies 4 transient states, Init (management initialization) state, Module PwrUp (module power up) state, PwrDn (module power down), and Resetting state. Transient states are introduced in module state machine to represent a time course when module completes a transition of its behavior between two steady states. This is of importance for providing host a signal indicating an indeterministic behavior of a module.

3.2.4.1 Reset State

While the precise behavior of Reset state varies with implementation, the TWI and all digital control logic are turned off, at least from MIS point of view. In general, the module is in its minimum low power state and the module is generally in a “dead state”. Reset state is entered by the assertion of MOD_RSTs.

Figure 8 Module State Transition Diagram



3.2.4.2 Init State

Upon the de-assert of MOD_RSTs, module enters tInit state. A required action of this transient state is to completely initialize the management logic and TWI. Memory map and internal registers that control the behavior of module shall be fully initialized with power on default values stored in “Module Boot Record”. Note these default values that control the hardware may not take effect so the module maintains in low power mode. Module exits from this state by completing the initialization process and reports its state transition in L00h.3 and generate an interrupt. Host intervention in this state shall be not effect.

3.2.4.3 LowPwr State

If MOD_LOWPWRs is asserted, module shall enter LowPwrstate which is a steady state. Module hardware and software behaviors are defined in Table 5. Important activities of host include reconfiguring the module, if power on default is not desired, and determining a module’s health condition. Module exits this state when MOD_LOWPWRs is de-asserted.

3.2.4.4 PwrUp State

Module enters this state upon the de-assert of MOD_LOWPWRs. This is the most important transient state within which all module level and lane level resources (hardware) shall power up to operating conditions. Module powers up these resources according to the default values stored in the Control Register Set (see 3.5.1), and other internal registers related to configuring the module according to the application selection codes. Upon

finishing the power up process, module shall “boot to configuration” and then exits to Ready State. An interrupt signal shall be asserted on exit.

Note that some initial values stored in the Control Register Set, such SI parameters, may need to be optimized again. During this transient state, Host is assumed to provide all the necessary idle packets or other types of training signals to each lane for such purpose.

3.2.4.5 Ready State

Module enters this state upon finishing module power up process. In Ready state all of the module level resources shall be in operation condition. All the lane level resources shall be in operation condition according to Control Register Set initialized in Init state or modified in LowPwr state. Module shall be in the condition to perform data transmission and reception for host with all the functions listed in Table 5 Module and Lane Behavior per State active.

Once module enters Ready state, any host lane or media lane can be powered on or off without affecting the state. Only LowPwrS or ResetS can bring module out of Ready State.

3.2.4.6 PwrDn State

Module enters this state upon the assert of MOD_LOWPWRs or MOD_RSTs. In this state, a module powers down all the power-consuming resources but maintain control logic and TWI fully functional.

3.2.4.7 Fault State

The Fault state is provided to indicate that a module fault has occurred. The Fault state shall only be entered when module detects a condition that could cause damage such as TEC runaway, flash corruption, etc. On entry to this state, a module shall immediately assert interrupt and enter low power mode.

In this state, module management interface and DDM shall remain fully functional. The module shall be put in low power mode to avoid the possibility of permanent module damage. Further diagnosis of the failure can be conducted by interrogating fault, alarm, warning, and status registers and other registers.

In this state, the PHYs are powered down and loop-back is not possible. The host outputs shall go to a steady state (no transitions).

Fault state is a steady state, and it shall exit to Reset state upon the assertion of MOD_RSTs.

Table 5 Module and Lane Behavior per State

MODULE RESOURCES/FUNCTIONS		UNDER MODULE STATE OF						
		Reset	**Init**	**LowPwr**	**PwrUp**	**PwrDn**	**Ready**	**Fault**
Module control	Reset pin	Effective	Effective	Effective	Effective	Effective	Effective	
	Soft reset	NA	NA	Effective	Effective	Effective	Effective	
	Low Power pin	No effect	No effect	Effective	Effective	Effective	Effective	

	Soft Low Power	NA	NA	Effective	Effective	Effective	Effective	
	Other hardware ModSel, TWI communication, Alarm/Warning masks, User EEPROM write	NA	NA	Effective	Effective	Effective	Effective	
Lane control	Lane power up, TX lane disable, TX EQ (CTLE), RX EQ	NA	NA	No effect	No effect	No effect	Effective	
	TX Rate/Application select	NA	NA	No effect**	Effective	No effect	Effective	
	RX Rate/Application select	NA	NA	No effect**	Effective	No effect	Effective	
	TX CDR Controls	NA	NA	No effect	Effective	No effect	Effective	
Module DDM	Module monitors, Module Alarm/Warning, IntL bit/pin, Module state/change	NA	NA	Active	Active	Active	Active	
TX DDM	TX monitors, TX alarm/warning	NA	NA	Inactive	Inactive	Inactive	Active*	
	TX LOS/LOL, TX summary. TX Fault	NA	NA	Inactive	Inactive	Inactive	Active	
RX DDM	RX monitors	NA	NA	Inactive	Inactive	Inactive	Active*	
	RX alarm/warning	NA	NA	Inactive	Inactive	Inactive	Active*	
	RX LOS/LOL, RX summary	NA	NA	Inactive	Inactive	Inactive	Active	
NA = Not applicable, Active* = Actively update for TX when TX disable is de-asserted or for RX when RX LOS is de-asserted, No effect** = Write has no immediate effect if Control Register Set is in Freeze mode, validation applies.								

3.3 Basic Digital diagnostic monitors (DDM)

3.3.1 Module Interrupt Signal (Pin and Bit)

ACMIS specifies the following fault, alarm, warning, status (FAWS) signal that contribute to generating an Interrupt, both at Pin and bit, to alert host an abnormal condition of the module. Logically, each of the FAWS source is subject to their respective mask bit and then logically OR together to trigger the interrupt.

Table 6 FAWS Signals Contributing to Interrupt

PAGE	BYTE/BIT	NAME	DESCRIPTION	NOTE
L00h	3.3~1	Module State		
	4~7	Bank n lane flag summary		
	8.0	L-Module state change flag		
	9~11	Latched alarms and warnings	Vcc, module temp, Aux1, Aux2, Vendor defined,	
U11h	132~133	Host/Media lane n Powered up Status	Trigger interrupt upon all lanes powered up and ready according to configuration. If lanes are configured to be powered down, they shall be excluded from this AND logic.	Configuration may set some lane to be powered done.
U11h	135~152	All lane FAWS latched		

When Interrupt alerts the Host a latched condition, the Host may query the latched registers for the condition. The latched bits are cleared on the read of the corresponding register. Thus, a read of all latched registers can be used to clear all latched register bits and to de-assert Interrupt.

3.3.2 Module Alarm/Warning Flag Conformance per State

Table 7 Module and Lane Flag Compliance to State describes the flag conformance for all module flags, per module state. In module states where a flag is indicated as 'Not Allowed', the module shall not set the associated flag bit while the module is in that state. All module flags shall be 'Not Allowed' throughout the Reset and Init states. Host implementers should note that if certain interrupts are undesirable, the host may mask those interrupts by setting the corresponding interrupt mask bit at any time after the management interface is initialized. The vendor-defined flag is Allowed in ModuleLowPwr and Fault if and only if it applies to a feature that is available in Low Power Mode.

Table 7 Module and Lane Flag Compliance to State

Flag	Page	Byte	State				
			LowPwr	PwrUp	Ready	PwrDn	Fault
Module state change	00h	8	Allowed	Allowed	Allowed	Allowed	Allowed
Module temperature	00h	9	Allowed	Allowed	Allowed	Allowed	Allowed
Vcc 3.3V	00h	9	Allowed	Allowed	Allowed	Allowed	Allowed
Aux1 – TEC Current if U01.145.0=1b.	00h	10	Not Allowed	Allowed	Allowed	Allowed	Allowed
Aux2 – TEC Current if U01.145.1=1b.	00h	10	Not Allowed	Allowed	Allowed	Allowed	Allowed
Aux2 – Laser temp if U01.145.1=0b	00h	10	Allowed	Allowed	Allowed	Allowed	Allowed
Aux3 – Laser temp if U01h.145.2=0b	00h	11	Allowed	Allowed	Allowed	Allowed	Allowed
Aux3 – Vcc2 if U01h.145.2=1b	00h	11	Allowed	Allowed	Allowed	Allowed	Allowed
Vendor-defined	00h	11	See below	Allowed	Allowed	Allowed	TBD
TX Fault	11h	135	Allowed	Allowed	Allowed	Allowed	Allowed
TX LOS	11h	136	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
TX CDR LOL	11h	137	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
TX Adaptive Input Eq Fault	11h	138	Not Allowed	Allowed	Allowed	Not Allowed	Not Allowed
Tx output power High Alarm	11h	139	Allowed	Allowed	Allowed	Allowed	Allowed
Tx output power Low alarm	11h	140	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx output power High warning	11h	141	Allowed	Allowed	Allowed	Allowed	Allowed
Tx output power Low warning	11h	142	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High Alarm	11h	143	Allowed	Allowed	Allowed	Allowed	Allowed
Tx Bias Low alarm	11h	144	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
Tx Bias High warning	11h	145	Allowed	Allowed	Allowed	Allowed	Allowed
Tx Bias Low Warning	11h	146	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
RX LOS	11h	147	Not Allowed	Allowed	Allowed	Allowed	Not Allowed
RX CDR LOL	11h	148	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed
RX Input Pwr High Alarm	11h	149	Not Allowed	Allowed	Allowed	Allowed	Not Allowed
RX Input Power Low alarm	11h	150	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed

RX Input Power High warning	11h	151	Not Allowed	Allowed	Allowed	Allowed	Not Allowed
RX Input Power Low warning	11h	152	Not Allowed	Not Allowed	Allowed	Not Allowed	Not Allowed

3.4 Application Select

Historically modules have single host media lane and the Application Select only involves data rate select and signal format select (see SFF-8079,8089). Contemporary modules are often constructed with multiple host lanes and media lanes, sometimes with electronic multiplexer ICs to merge multiple host lanes into single or more media lanes (gearbox case). Therefore, the definition of Application shall be extended to the single lane Application assigned to multiple host lanes and media lanes. ACMIS specifies the data structures and methods needed for the new Application Select in this section.

3.4.1 Application Selection Advertisement

ACMIS specifies three data constructs for Multilane Application Selection,

1) One Module PMD Type Register
2) Two Lane Map Registers for a Module PMD Type (Lane Map for short),
3) Application Selection Table which contains 1 or more Application Selection Codes (AppSel for short). Each AppSel Code points to a combination of Host Electrical Interface Code and Module Media Interface Code (Host/Media Interface Code) a module supports. The maximum number of AppSel Code is 32.

Note that Host Electrical Interface Code and Module Media Interface Code are established in the recent work of CMIS 3.0 (as well as in SFF-8024 WIP). It combines data rate, signal format, required lane counts, and other information together to support contemporary modules.

3.4.1.1 Module PMD Type Advertisement

Both DSFP Module Specification (Rev. 1.0) and OSFP MSA Specification (Rev. 1.93) specifies typical Module Optical PMD block diagrams (This topic is related to the topic of “Extended Specification Compliance Codes” in SFF-8024 which is to be updated to include the latest 400G modules). These diagrams define typical module PMD structures such as host/media signal rate/format, host/media lane mapping, etc. in the context of reach spec of CR, DR, FR, LR and other variations.

ACMIS allocates U01h.163 as the register of Module PMD Type Code pointing to a particular Module Optical PMD Block Diagrams. Appendix A contains detailed description of each Module PMD Type for multiple form factors, extracted from respective MSA’s (DSFP and OSFP in the current Rev.).

Module shall advertise this Code to indicate the module PMD structure. Vendor shall use the information in Appendix A to program register U01h.163.

3.4.1.2 Module Lane Map Advertisement

ACMIS allocates two registers U01h.164~165 to encode the Lane Map for a Module PMD Type. The below Table 8 Examples of DSFP/OSFP Module Lane Map uses the information extracted from Module PMD Type diagrams in Appendix A. Note this advertisement method is suitable to any 2-lane, 4-lane, 8-lane modules. For modules that have more than 8 lanes, Bank Select is used and the same lane map between banks is assumed. If not the case more bytes can be allocated for it.

ACMIS specifies several additional rules for lane map advertisement.

1) Enumerate both host lane and media lane sequentially. If a module has 8 host lanes and 4 media lanes (e.g. a DR4 module), the host lane shall be assigned with lane numbers 1, 2, …, 8, while media lanes shall be assigned with lane numbers 1, 2, 3, and 4.
2) If an Application involves minimum number of host lanes and media lanes, it is called minimum configuration of Application. For example, in a DR4 module, a minimum Application involves two host lanes and 1 media lane. A module may contain multiple minimum Applications. For example, a DR4 module contains 4 minimum Applications.
3) In a minimum Application, the lane with smaller lane number is the leading lane and the other lanes are trailing lanes. In the above example, host lane 1 is the leading lane and host lane 2 is the trailing lane.
4) In a minimum application, the media lane is always associated with the leading host lane. This rule is related to assigning Application Selection Code to a minimum Application specified in next section.

Table 8 Examples of DSFP/OSFP Module Lane Map

MODULE PMD TYPE	PMD TYPE CODE	REGISTER	LANE	1	2	3	4	5	6	7	8
			Bit	0	1	2	3	4	5	6	7
DSFP Parallel Fiber 100GBASE-SR2	3	U01h.164	Host Lane	1	1	0	0	0	0	0	0
		U01h.165	Media Lane	1	1	0	0	0	0	0	0
DSFP 2:1 Mux and 50GAUI-2: 50GBASE-SR	5	U01h.164	Host Lane	1	1	0	0	0	0	0	0
		U01h.165	Media Lane	1	0	0	0	0	0	0	0
OSFP Parallel 400G SR8	3	U01h.164	Host Lane	1	1	1	1	1	1	1	1
		U01h.165	Media Lane	1	1	1	1	1	1	1	1
OSFP Parallel SMF 400GBASE-DR4	4	U01h.164	Host Lane	1	1	1	1	1	1	1	1
		U01h.165	Media Lane	1	0	1	0	1	0	1	0

Notes: What host can learn from this table,

1) Number of host lanes exists by counting the 1's,
2) Minimum app configuration. For example, for DSFP Type 3, it is 1:1. For OSFP Type 4, it is 2:1.
3) Leading lane position. For example, for DSFP Type 3, it is lane 1 and 2 for 2 minimum apps. For OSFP Type 4, App leading lanes are 1, 3, 5, 7.
4) Maximum number of applications supported. For example, for DSFP Type 3, it is 2. For OSFP Type 4, it is 4.

3.4.1.3 Application Selection Advertisement

ACMIS allocates Page U04h for advertising AppSel Code a module supports, with following elements,

1) U04h.128 indicates number of AppSel Codes a module supports,

2) U04h.129 indicates media type number selecting multiple Media Interface Tables in Appendix B.
3) U04h.130~193, the Application Selection Table, containing 1 to 32 AppSel Code with each Code pointing to a combination of Host Electrical Interface Code and Module Media Interface Code.

Table 9 Examples of AppSel Code Advertisement illustrates how Application Selection Table Code information is used to compose AppSel Code for one or more Applications supported by a specific module.

Table 9 Examples of AppSel Code Advertisement

MODULE TYPE	APPSEL CODE	BYTE ADDR.	HOST/ MEDIA I/F CODE	DESCRIPTION	DATA RATE APP/SIGNAL	LANE COUNT	MODU-LATION
2-Lane 100GBASE-DR Application Advertising Example							
2-Lane 2:1 Mux &100GAUI-2: 50GBASE-DR	1	U04h.130	0Dh	100GAUI-2 C2M	106.25 / 26.5625	2	PAM4
		U04h.131	14h	100GBASE-DR			PAM4
2-Lane 100GBASE-SR2	1	U04h.130	0Ah	50GAUI-1 C2M	53.13 / 26.5625	1	PAM4
		U04h.131	07h	50GBASE-SR	-	1	PAM4
400GBASE-DR4 Application Advertising Example							
8-Lane DR4	1	U04h.130	11h	400GAUI-8 C2M	425.00 / 26.5625	8	PAM4
		U04h.131	1Ch	400GBASE-DR4	425.00 / 53.125	4	PAM4
	2	U04h.132	0Dh	100GAUI-2 C2M	106.25 / 26.5625	2	PAM4
		U04h.133	14h	100GBASE-DR	106.25 / 53.125	1	PAM4
400G-SR8 Transceiver Application Advertising Example							
8-Lane 400G-SR8	1	U04h.130	11h	400GAUI-8 C2M	425.00 / 26.5625	8	PAM4
		U04h.131	10h	400G-SR8	-	8	PAM4
	2	U04h.132	0Fh	200GAUI-4 C2M	212.50 / 26.5625	4	PAM4
		U04h.133	0Eh	200GBASE-SR4	-	4	PAM4
	3	U04h.134	0Dh	100GAUI-2 C2M	106.25 / 26.5625	2	PAM4
		U04h.135	0Ch	100GBASE-SR2	-	2	PAM4
	4	U04h.136	0Ah	50GAUI-1 C2M	53.13 / 26.5625	1	PAM4
		U04h.137	07h	50GBASE-SR	-	1	PAM4
8x50G AOC Application Advertising Example							
8-Lane 8x50G AOC	1	U04h.130	11h	400GAUI-8 C2M	425.00 / 26.5625	8	PAM4
		U04h.131	03h	AOC BER<2.4e-4	-	8	PAM4
	2	U04h.132	0Fh	200GAUI-4 C2m	212.50 / 26.5625	4	PAM4
		U04h.133	03H	AOC BER<2.4e-4	-	4	PAM4

3.4.1.4 Inter-lane clock dependency

Because of IC implementation limitation, inter-lane clock dependency may exist while it is assumed each lane can be clocked independently. Register U01h.164, Inter-lane Clock Dependency is allocated to advertise possible clock dependency exceptions. Note that clock dependency between lanes imposes additional constraint in configuring a module into multiple applications. For example, a module has 4-lane clock dependency, that is, clock much be the same for lanes 1~4 and for lanes 5~8. It is not possible to have an application

with data rate of 10G over lanes 1 and 2, and a second application with data rate of 25G over lanes 3 to 4, due to the clock dependency.

3.4.2 Application Select Method

ACMIS allocates 8 registers U10h.178~185 for Application Select. ACMIS also defines a set of special AppSel codes and methods for Application Select and placement of multiple Applications in a module.

3.4.2.1 Special AppSel Codes

A multilane module may run multiple Applications. To place multiple Applications special codes shall be defined to facilitate module vendor and user to make Application placement compatible with module PMD Type and Lane Map. Table 10 Special AppSel Codes for Application Placement lists these codes and there usage.

Table 10 Special AppSel Codes for Application Placement

APPSEL CODE (HEX)	DSCRIPTION	ACCESS	POWER-ON DEFAULT
00h	Indicating a lane is not implemented.	RO	00h
01h~20h	Normal AppSel code to assign an application to a host lane and corresponding media lane. This code is selected from Application Selection Table in U04h. These codes can be programmed in Application Select Registers either by vendor or user.	R/W	Per vendor
21~EFh	Reserved		
F0h	Indicating this is a trailing lane of a multilane application and this lane uses the same AppSel code as the leading lane with smaller lane number.	RO	F0h
F1h	Indicating this is a trailing lane of a multilane application and this lane uses the same AppSel code as the leading lane with smaller lane number. Note that F1h is different from F0h that it indicates it is writable by user	RW	F1h
F2h	Indicating this is a trailing lane of a multilane application and this lane uses the same AppSel code as the leading lane with larger lane number.	RO	F2h
F3h	Indicating this is a trailing lane of a multilane application and this lane uses the same AppSel code as the leading lane with smaller lane number. Note that F3h is different from F2h that it indicates it is writable by user	RW	F3h
F1h~FFh	Reserved		

3.4.2.2 Application Select Method

1) Write AppSel Codes to the registers corresponding to the leading host lanes. The Host Electrical Interface Code applies to the host lane and Module Media Interface Code applies to the leading lane associated media lane.
2) Write special code “F0h” or “F2h” to all the trailing lane registers, depending upon the choice of leading lanes.
3) Either “F0” or “F2” shall be read-only. Vendor shall use these codes to registers corresponding to a trailing lane such that a multilane Application is indicated.
4) Write special code “F1h” or “F3h” to all the trailing lane registers, depending upon the choice of leading lanes. Note this method is different from above that F1h and F3h are overwritable by vendor and user when the lane is a leading lane but needs to be programmed as a trailing lane to use the same AppSel code as the leading lane further down the direction. This approach shall be used to indicate multiple

leading lanes are used for a single Application (a link). For example, 4 host lanes and 2 medias lanes can be grouped together as one application.

5) Write special code "00h" indicates the corresponding lane is not implemented. In a 2-lane module like DSFP, registers corresponding to lanes 3~8 shall be written with 00h.
6) In a custom configuration, register Clock Dependency shall be used to determine its constraints. Module vendor can use special code "F0h" or "F2h" to enforce such constraint.

Application Select for a typical DSFP DR is exemplified in the following table.

Table 11 Example of DSFP Application Configurations

APPLICATION	APP SEL CODE	APPLICATION SELECT REGISTER ON PAGE U10H							
		178	179	180	181	182	183	184	185
DSFP 100GAUI-2:100G-SR2	01h*	01h	F0h	00h	00h	00h	00h	00h	00h
DSFP Dual Port: 50GBASE-SR, (breakout apps)	02h*	02h	02h	00h	00h	00h	00h	00h	00h
2:1 Mux and 50GAUI-2: 50GBASE-FR	03h*	03h	F0h	00h	00h	00h	00h	00h	00h

"*" indicates the numbers are arbitrarily defined in Application Selection Table.
Notes:
1) Normal AppSel codes (1 ~ 32) indicates these are leading lanes that can be programmed by user.
2) Code "F1h" indicates these are leading lanes but programmed as trailing lanes to run the same AppSel code as the leading lanes at left. F1h code also indicates these registers are overwritable to reprogram.
3) Code "00h" indicates AppSel code is not present. In this case lane does not exist.

Application Select for a SR8 module is exemplified in Table 12 Typical SR8 Module Application Selection Placement Example. In this case, both single Application and multiple Applications (breakout) are illustrated. Note if rule 6) applies when SERDES ICs in the Custom Applications 02h and 03h (last row), then register 184 shall be programmed with "FAh" to indicate that lanes 5~8 can only operate on one clock rate.

Table 12 Typical SR8 Module Application Selection Placement Example

APPLICATION	APP SEL CODE	PER LANE APPLICATION SELECT REGISTER ON U10H							
		178	179	180	181	182	183	184	185
OSFP 400GAUI-8:400G-SR8	01h	01h	F1h	F1h	F1h	F1h	F1h	F1h	F1h
OSFP 2x 200GAUI-4:200GBASE-SR4, breakout	02h	02h	F1h	F1h	F1h	02h	F1h	F1h	F1h
OSFP 4x 400GAUI-2:400GBASE-SR2, breakout	03h	03h	F1h	03h	F1h	03h	F1h	03h	F1h
OSFP 8x 50GAUI-1:50GBASE-SR, breakout	04h	04h	04h	04h	04h	04h	04h	04h	04h
Custom 1x 02h App + 2x 03h App, 3 apps total.	02h, 03h	02h	F1h	F1h	F1h	03h	F1h	03h	F1h

1) Normal AppSel codes (1 ~ 32) indicates these are leading lanes that can be programmed by user.
2) Code "F1h" indicates these are leading lanes but programmed as trailing lanes to run the same AppSel code as the leading lanes at left.
3) F1h code also indicates these registers are overwritable to reprogram.

A DR4 module example is illustrated in Table 13 Typical DR4 Module Application Selection Example. Note that the green color marked cells are vendor defaults that are read only for indicating these are corresponding to trailing lanes. Other cell with FAh code can be overwritten when host desires to change the breakout applications.

Table 13 Typical DR4 Module Application Selection Example

APPLICATION	APP SEL CODE	PER LANE APPLICATION SELECT REGISTER ON U10H							
		178	179	180	181	182	183	184	185
400GAUI-8:400GBASE-DR4	01h	01h	F0h	F0h	F0h	FAh	F0h	FAh	F0h
4x100GAUI-2: 100GBASE-DR Breakout	02h	02h	F0h	02h	F0h	02h	F0h	02h	F0h
2x 200GAUI-4: 200GBASE-DR2 Breakout	03h	03h	F0h	FAh	F0h	03h	F0h	FAh	F0h
Custom 2x 02h App + 1x 03h App, 3 apps total.	02h, 03h	02h	F0h	02h	F0h	03h	F0h	FAh	F0h

1) Normal AppSel codes (1 ~ 32) indicates these are leading lanes that can be programmed by user.
2) Code F0h indicates trailing lanes programmed by vendor, cannot be changed in field according the lane map.
3) Code "F1h" indicates these are leading lanes but programmed as trailing lanes to run the same AppSel code as the leading lanes at left.
4) F1h code also indicates these registers are overwritable to reprogram.

3.4.3 Summary of Module Application Selection

With the data structures and rules defined above, ACMIS supports point-to-point applications, multiple applications, breakout applications, as well as imposing inter-lane clock dependencies, all with correctly writing Application Selection Codes and Special Codes in Application Select Registers U10h.178~185.

3.5 Module Configuration and Module Boot Record

To provide desired service to host a module shall be configured properly and completely for all its internal variables, including most of the VRs that control the module. A module shall be powered up to its configured state every time, whether through hardware or software power up process. Furthermore, methods and processes shall be specified for host to create, recall, store multiple desired configurations.

ACMIS specifies mechanisms to support above objectives by data structures, data flow, initialization of VR's, and the management of these elements.

3.5.1 Control Register Set, Module Boot Record, and Boot Record Manager

ACMIS specifies three data structures to support module startup process, module configuration, and in-service module management.

1) Control Register Set, a collection of module level and lane level control registers in both page L00h and U10h. These registers configure module resource to specified applications including the setup of IC's, photonics, signal integrity parameters, lane functions, etc. This register collection is specified in Table 14 Registers in Module Control Set. Note in the Control Register Set, ACMIS specifies every lane to have its own AppSel Code as part of the Application Select. This allows host to arbitrarily assign and change Application configurations.
2) A "Boot Record" (BR) containing all the INITIAL values of Module Control Set, stored in NVR. A minimum 1 to maximum 32 Boot Records are specified by ACMIS for each module and hence the same number of configurations.
3) A Boot Record Manager (BRM) register to manage the data flow between host, Control Register Set, and Module Boot Records, located at L00h.38.

Table 14 Registers in Module Control Set

PAGE	BYTE(S)	DESCRIPTION	NOTE
L00h	28	Squelch control, ForceLowPwr, SW reset	
L00h	31~34	Various masks	
L00h	126~127	Bank and Page Select	
U10h	Whole page	- Lane power up control for each lane - All CDR controls, - Application Selection for each lane - Tx Input equalization codes for both manual and adaptive control - Tx CDR control - Rx Output equalization codes for both pre-cursor and post-cursor - Rx CDR control and Amplitude control.	

ACMIS allocates half of 32 Boot Records as module vendor default configurations and the other half for customer to store their own MBR's. Through individual arrangement between customer and vendor, these numbers can be customized. Vendor default MBR's shall be optionally password (user password) protected to prevent accidental overwrite in the field.

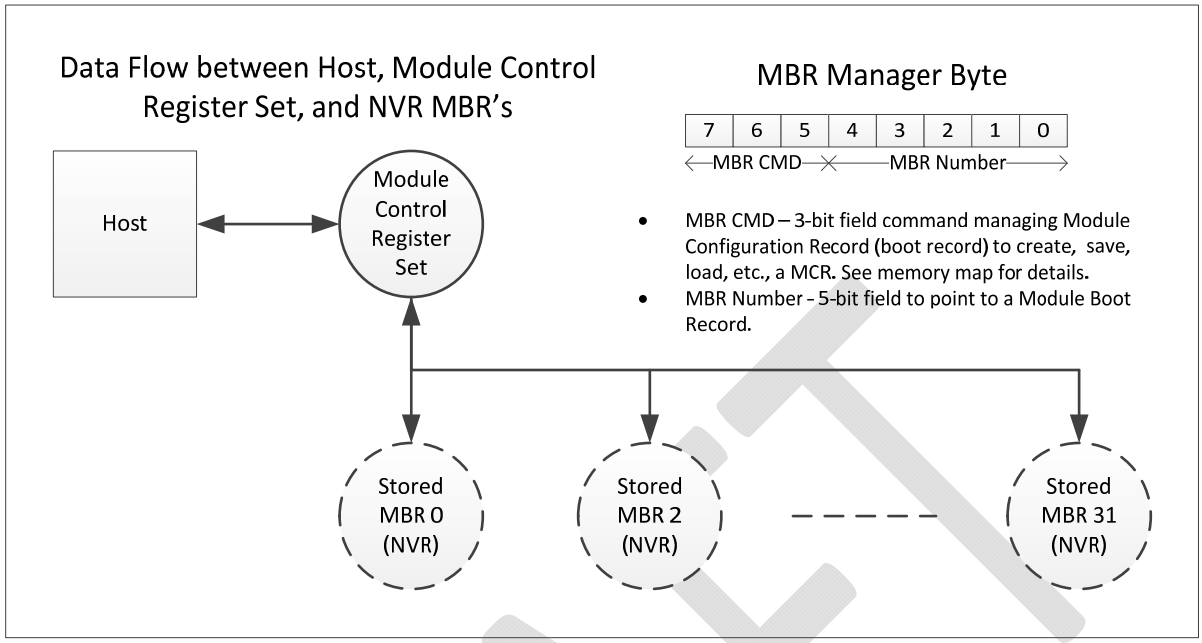
3.5.2 Module Boot Record Manager

The Boot Record Manager byte consists of two bit-fields, bits 7~5 for BRM CMD and bits 4~0 for MBR Number. Figure 9 Control Set Buffer Management illustrates the data flow between host, Control Register Set, and Save Boot Records. The following functions can be executed with Control Register Set, Module Boot Record Manager byte,

1) Freeze the update from Control Register Set to hardware, allowing host to edit the content Control Register Set.
2) Load a MBR at MBR number to refresh the content of Control Register. Note these loaded contents shall not take effect if Freeze Control Register Set has been issued.
3) Save the edited content of Control Register Set into a MBR with MBR number.
4) Assign an existing MBR as the next time power on default configuration.
5) Un-freeze the update from Control Register Set to hardware – to apply the content of Control Register Set immediately. In this mode, write to Control Register Set shall also take effect immediately.

Command details are listed in Description column of L00h.38.

Figure 9 Control Set Buffer Management



3.5.3 Software Initialization

To start a module with software initialization, host shall assert LowPwr pin before module plugged in or Vcc available, module shall boot into LowPwr state with Module Control Register Set initialized by values from default MBR and then wait for host intervention. In LowPwr state host can verify the power class of the module, adjust any settings from default values, editing new or custom MBR's, and other management tasks. Before host de-asserting LowPwrS signal, host shall provide signals to each host lane for SI parameter optimization. Upon host de-asserting LowPwrS signal, module shall enter PwrUp state using default SI parameters. If re-training is desired, host shall provide proper training signals and de-freeze the Control Register Set. Upon the module finishing power up process, module shall signal host with interrupt signal and set all Lane Power up and Ready flags. Module enters Ready State.

3.5.4 Hardware Initialization

To power up a module with hardware initialization, host shall provide Vcc, and de-assert Low Power pin prior to module present signal detected and then feed signals to each host lane for module SI parameter adjustment. Then host shall de-asserted ResetS signal. Module shall enter Init state and initialize Module Control Register Set with initial values from the default Module Boot Record. Module shall then go through LowPwr state and enter PwrOn state, executing power on sequence and using default values of SI parameters from the Boot Record. Module shall signal the successful initialization, module power up, and lane power up by asserting all Lane Power up and Ready flags and generating an interrupt. Module shall enter Ready state.

Should host desire to retrain equalizer coefficient in Ready state, host shall provide training signals to one or more host lanes that involved in the Applications to be reinitialized and un-freeze Module Control Register Set. Module shall reset the Lane Power up and Ready flags. Upon successful lane power up and SI parameter training, module shall assert all Lane Ready flags (U11h.133~134) to indicate the completion of SI retraining and ready for operation.

Note in both cases, once module enters Ready state, individual lanes can be powered on and off without affecting Ready state.

3.6 Command and Data Block (CDB)

Editor's note: CDB detail is under discussion with CMIS advisor group. Suggest delaying the implementation, including firmware upgrade feature and PRBS feature.

While memory map in general provides a directly readable and writable interface, it requires tedious operation and maintenance. It is difficult to transfer ad-hoc data and to execute batch commands. It is a benefit to have a memory map compatible and shared data block with secured error checking and handshaking to serve new applications. Command-and-Data Block (CDB) is introduced in ACMIS for such purpose. Another motivation of using CDB is to provide a handshaking mechanism for host to gain feedback from a module for command execution and data transfer. It presents to the host the same set of registers interface for different applications and meantime it reliefs the module from the burden of maintaining the growing number of registers.

3.6.1 CDB Implementation

ACMIS allocates Upper Page 9Fh as the Command and Data Block (CDB) page by referencing similar concept deployed in CFP MSA MIS. CDB consists of a CDB Reply (RPL) byte, a CDB Command (CMD) byte, a Payload length byte (LEN), CDB CRC, and CDB Data Payload (PL) as a universal mechanism for large size data exchange between host and module with secured handshaking. Table 27 U9Fh (15) Command and Data Block specifies the details of CDB.

3.6.2 CDB Reply Byte

The CDB Reply byte consists of two bit-fields, the CDB Status (bits 7~6) and CDB Message (bits 5~0). STS Status indicates whether module is ready to receive a write from host or it is busy in processing a previous write. Meanwhile it indicates the outcome of execution result of a previous write, success or failure. STS Message field provides detailed information to the execution of previous write. In this current rev. of ACMIS, Byte 37 is allocated for implementing WFC. The details of STS Status and Message are listed in Table 15 CDB STS Details.

Table 15 CDB STS Details

BYTE ADDR	SIZE	BIT	ACCESS	REGISTER NAME	DESCRIPTION	INIT. VALUE

37	1		RO	CDB Reply	STS register controls the write flow from host to module. Registers under STS are marked. The whole CDB is under WFC.	00h
		7	RO	Status (STS)	One-bit value indicating the availability of module writable status. 0: Module Idle, host can write, 1: Module busy, host needs to wait.	
		6	RO	Last CMD Result	0: Last write or command completed successfully, 1: Last write or command failed.	00b

		5~0	RO	Last CMD Message	An 6-bit value coding STS Message related to each STS Status.
					If STS Status = STS Idle, then
					00h: Reserved,
					01h: Ready to accept host command,
					02h~2Fh: Reserved by MSA,
					30h~3Fh: Allocated for vendor use.
					If STS Status = Command in Progress, then
					00h: Reserved,
					01h: Command is captured but not processed,
					02h: Command checking is in progress,
					03h: Command execution is in progress,
					04h~2Fh: Reserved by MSA,
					30h~3Fh: Allocated for vendor use.
					If STS Status = STS Command Completed Successfully, then
					00h: Reserved,
					01h: Command completed successfully without specific message,
					02h~1F: Reserved by MSA,
					20h~2Fh: For individual STS Command or task progress report,
					30h~3Fh: Allocated for vendor use.
					If STS Status = Command Failed, then
					00h: Reserved,
					01h: Unknown command,
					02h: No detail.
					03h: Reserved,
					04h: Command checking time out, indicating the module command checking time is longer than 150 ms,
					05h: CRC error,
					06h: Password error,
					07h~0Fh: Reserved for STS command checking error,
					10h~1Fh: Reserved by MSA
					20h~2Fh: For individual STS command or task error,
					30h~3Fh: Allocated for vendor use.	

3.6.3 Application of CDB

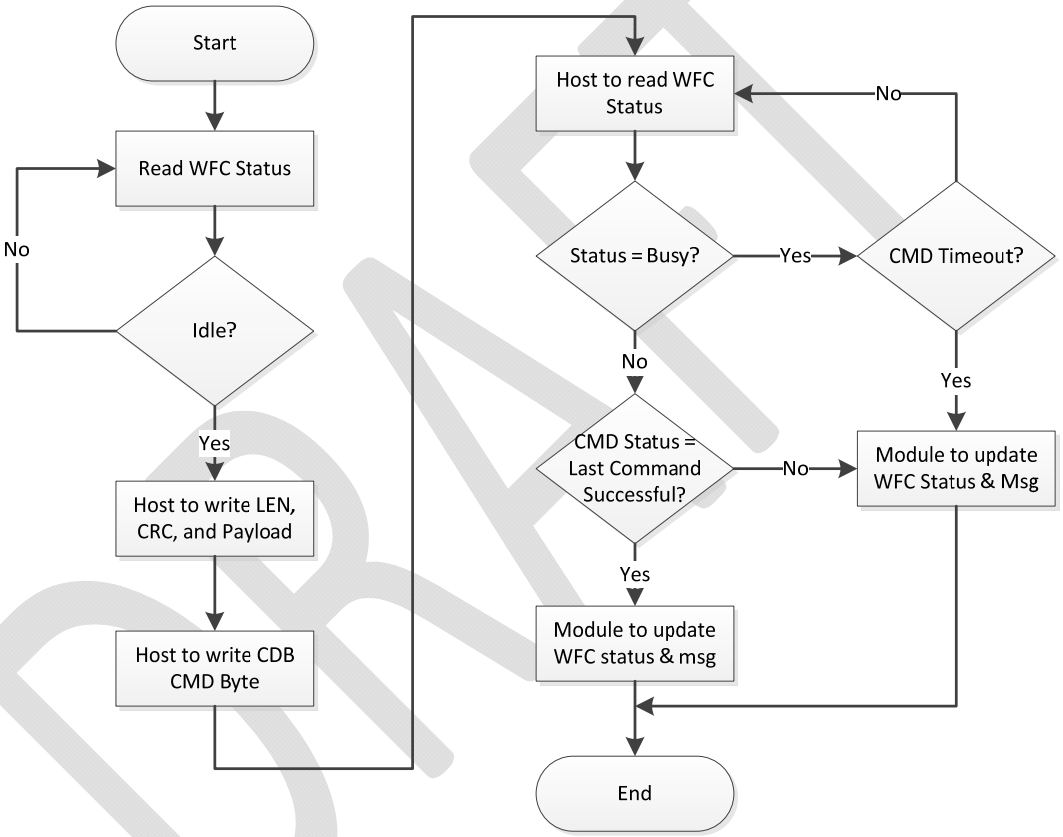
CDB takes the format of a block of registers and it is fully compatible with existing memory map structure. The same block of registers can be employed with various command and data as a common application programming interface (API) of a module. By defining a set of commands with proper data, complex applications can be executed with clear procedure and handshaking. Some applications of CDB include,

1) Password entry and change with confirmation,
2) Configuring host and media lanes for an application or apply a Staged Control Set,
3) Bulk data transfer.

3.6.4 Command Execution

Host shall start a CDB command by reading the Status byte at U0Fh.128 to confirm CDB is in Idle state. Host shall write the payload data, LEN byte, CRC bytes in any order. The last byte to write shall be CDB CMD. By writing CDB CMD byte host commits to the LEN, Payload, and CRC and triggers module to execute the command with or without the associated payload data. If a reply is expected host shall read STS to detect the status of command execution. Figure 10 CDB Command Execution Flow details the CDB command execution flow.

Figure 10 CDB Command Execution Flow



3.6.5 Basic CDB Commands

Table 16 CDB Command Table lists some common CDB commands for host to write to module with secured handshaking.

Table 16 CDB Command Table

CMD Code	Command Name	Payload Size	Pass-word	Description
00h	Reserved			
System Command				

CMD Code	Command Name	Payload Size	Pass-word	Description
01h	Enter Password	2	N	Optional method of entering password with a CDB Reply message to confirm the acceptance of password entered with the payload of this command. Payload: PS = 2; PL0 = Most significant word of password, PL1 = Least significant word of password, Expected CMD specific Reply: 0140h: Password ok, 0340h: Password failure, 0341h: Other errors.
02h	Save New Password	2	Y	Alternative method of entering and saving a new password with a CDB Reply message to confirm the acceptance of a new password entered with the payload of this command. Payload: PS = 2, PL0 = Most significant word of a new password PL1 = Least significant word of a new Pass word. Expected CMD specific Reply: 0140h: New password saved, 0340h: New password save failed, 0341h: Other errors.
03h	Enable Password	0	N	Enable the optional password protection.
04h	Disable Password	0	Y	Disable the optional password protection.
05h	Enable CDB CRC	0	N	Enable the optional CRC for CDB. This Command is volatile after power cycle. No CRC checking shall be executed on this command itself, but CRC shall take effect starting from next CDB Command/Reply Frame if this command is executed successfully.
06h	Disable CDB CRC	0	N	Disable the optional CRC for CDB. CRC checking shall be performed for this command itself, but CRC shall be inactive starting from next CDB Command/Reply Frame.
Register Access Commands				
11h	Multiple Register Read	2	Y	Host to read multiple registers with one command. PS = total size of payload. PL0=Bank Select, PL1=Page Select, PL2 = initial address, PL3= number of register to read counting from initial address. If number of register exceeds the page boundary, module shall stop at the page boundary and return adjusted payload length.
12h	Multiple Register Write	L+2	Y	Host to write L registers. PL0=Initial address, PL1=number of register to write, PL2 and on: register content.
13h	Bulk Data Read	1	Y	Host to read L registers from module. PL0=Bulk data batch number or a descriptor specified by vendor.
14h	Bulk Data Write	L+1	Y	Host to write L registers to module. PL0=Bulk data batch number or a descriptor specified by vendor.
15h	Selected Register Read	2*L+1 or 3L+1	Y	Host to read a set of L registers at specified addresses. PL0 = Read_Type. If Read_Type = 2, Read uses two-byte address, Page number and byte addr. Module shall return maximum 61 bytes data. If Read_Type = 3, Read uses three-byte addresses, Bank, Page, and Byte. Module shall return maximum 40 bytes of data. PL0 = 0, 1, and 4 to 255 are reserved. No space is allowed between addresses and data.
16h	Selected Register Write	3L+1 or 4L+1	Y	Host to write a set of L registers to module at specified addresses. PL0= Write_Type. If Write_Type = 2, Write uses 2-byte address (Page and Byte) plus the data byte. The maximum data can be written is 40. If Write_Type=3, Write uses 3-byte address (Bank, Page, and Byte) plus the data byte. The maximum data byte can be written is 30. No space is allowed between addresses and data.

CMD Code	Command Name	Payload Size	Pass-word	Description
17h	Module DOM Max/Min Value Block Read	1	Y	Read all media lane DOM data of all banks. Returned data shall be in the order of lane n, n = bank*8 + k, where k = 1, …, 8; bank = 0, 1, …. All the data shall be in big endian order, Max value followed by Min value since last time read. two bytes each. Command Payload: PL0 has a value to indicate which DOM variable to read. 0: Reserved, 1: Tx bias, 2: Tx power, 3: Rx power, 4: Module temperature (2 bytes) 5: number of Laser temperature in each module (1 byte), followed by laser temperatures, 6~9: reserved, 10: All the above. Note that host shall count the total bytes returned by module and considering the total lanes in a module. 5: Module temperature Reply Payload shall contain all the data this Command requested. Reply Message: Generic.

1

4 FEATURED APPLICATIONS

4.1 PRBS Test

Editor's note: CDB detail is under discussion with CMIS advisor group. Suggest delaying the implementation, including firmware upgrade feature and PRBS feature.

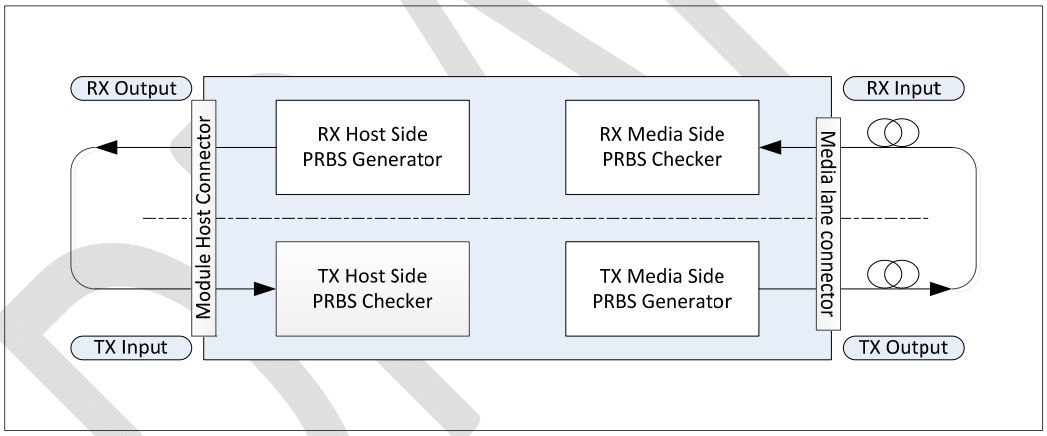
4.1.1 PRBS Test Overview

ACMIS specifies the support to this function including,

- PRBS function advertisement registers in Page 01h, 163~175 (TBD)
- PRBS function control registers (Page 1Ch)
- PRBS pattern select registers (Page 1Ch),
- PRBS data bit counters (Page 1Ch),
- PRBS error bit counters (Page 1Ch),
- PRBS function for both Host and Media size,
- An Ad-hoc floating number format for data bit and error bit counters.

4.1.2 Host/Media Lane PRBS Setup

Figure 11 Module Built-in PRBS Components and Test Signal Flow (1-lane shown)



4.1.3 Host/Media Lane BER Calculation

Upon assertion of RX PRBS Enable bit Module shall automatically set the Media Lane PRBS Data Bit Count and Media Lane PRBS RX Error Count (each per lane) to zero and shall start the accumulation. Module shall stop the accumulations for both data bit counting and error bit counting after RX PRBS Checker Enable is de-asserted. The counts shall be kept unchanged until RX PRBS Checker Enable is asserted next time.

The Host can read the Media Lane PRBS Data Bit Count and the per-lane Media Lane PRBS RX Error Count at any time. The bit error rate (BER) can be calculated by simply dividing the RX error count by data bit count. To achieve an accurate BER calculation, it is recommended that the Host reads these registers after PRBS Enable is de-asserted.

Both Media Lane PRBS Bit Count and Media Lane PRBS Error Count registers use an ad-hoc floating data format with 6-bit unsigned exponent and 10-bit unsigned mantissa. While the maximum count of this ad-hoc floating-point number is 1023*2^63 ~= 2^73, MODULEMSA specifies the effective maximum count to be 2^64 – 1 with a precision of 1/1024 in using this ad-hoc data format. Some examples in this data format are listed Table 17 Ad-hoc Floating-Point Number Examples.

Table 17 Ad-hoc Floating-Point Number Examples

Count N (integer)	Mantissa (M)	Exponent (E)	Value Expression
0 ~ 1023	N	0	N * 2^0
1024 ~ 2047	N/2	1	(N/2) * 2^1
2048 ~ 4095	N/4	2	(N/4) * 2^2
4096 ~ 8191	N/8	3	(N/8) * 2^3

4.2 DOM MAX/MIN Value Read

DOM Max/Min value detecting and replying allows host to read DOM maximum and minimum values in between intervals of “Round-Robin” reads with multiple installed modules. Command 17h details the syntax in Table 16 CDB Command Table. If this feature is advertised by module vendor, module shall support Max/Min value detection between two reads of DOM values by host. Max/Min values shall be clear-on-read.

4.3 Firmware Field Upgrade

Editor’s note: CDB detail is under discussion with CMIS advisor group. Suggest delaying the implementation, including firmware upgrade feature and PRBS feature.

Host needs to issue a set of command to apply firmware upgrade process. Table 19 Firmware Upgrade Commands lists commands defined for firmware upgrade.

There should be at least two images available in a module if the firmware upgrade is supported. Image A should be factory default which should not be touched by firmware upgrade. Firmware download to image A should be rejected by the module. Firmware upgrade image should go to image B. Firmware upgrade image file should be a binary file. The firmware upgrade process is showed in Figure 12 Firmware Upgrade Process.

4.3.1 Firmware Image File Format and Content

The firmware file shall consist of two parts, a file header of 256 bytes of ASCII code and an image body of binary code. The file header shall contain the following text.

Table 18 Firmware Upgrade Image File Header

BYTE	SIZE	FIELD NAME	DESCRIPTION
0	16	Prompt for transceiver ID	Should have 16-byte string "Transceiver ID: "
16	2	Transceiver ID	Two ascii digits of the hex value of transceiver ID (read from byte 0 of the module).
18	2	Return	Carriage Return (0x0D) + New Line (0x0A)

20	13	Prompt for vendor name	Should have 13-byte string "Vendor name: "
33	16	Vendor name	16-byte Vendor name that matches content of module's vendor name field at page 00H, 129~144
49	2	Return	Carriage Return (0x0D) + New Line (0x0A)
51	12	Prompt for vendor OUI	Should have 12-byte string "Vendor OUI: "
63	8	Vendor OUI	Vendor OUI in format of "AA-BB-CC". AA, BB, CC are the ascii code of three-byte vendor OUI at page 00H, 145~147.
71	2	Return	Carriage Return (0x0D) + New Line (0x0A)
73	20	Prompt for vendor part number	Should have 13-byte string "Vendor part number: "
93	16	Vendor part number	Vendor part number to match content in module's page 00h, 148~163
109	2	Return	Carriage Return (0x0D) + New Line (0x0A)
111	8	Prompt for FW revision	Should have 8-byte string "FW Rev: "
119	7	FW Revision	New firmware revision up to 7 bytes with format MMM.NNN
126	2	Return	Carriage Return (0x0D) + New Line (0x0A)
128	6	Prompt for Date	Should have 6-byte string "Date: "
134	8	Date of this new firmware rev	Date with format "YY-MM-DD".
142	2	Return	Carriage Return (0x0D) + New Line (0x0A)
144	17	Prompt for Vendor Specific	Should have 17-byte string "Vendor Specific: "
161~ 253	92	Vendor specific	Add vendor specific comments/descriptions.
254	2	Return	Carriage Return (0x0D) + New Line (0x0A). If these two bytes are set to spaces (0x20), another 256 bytes follwed are used for vendor specific usage.

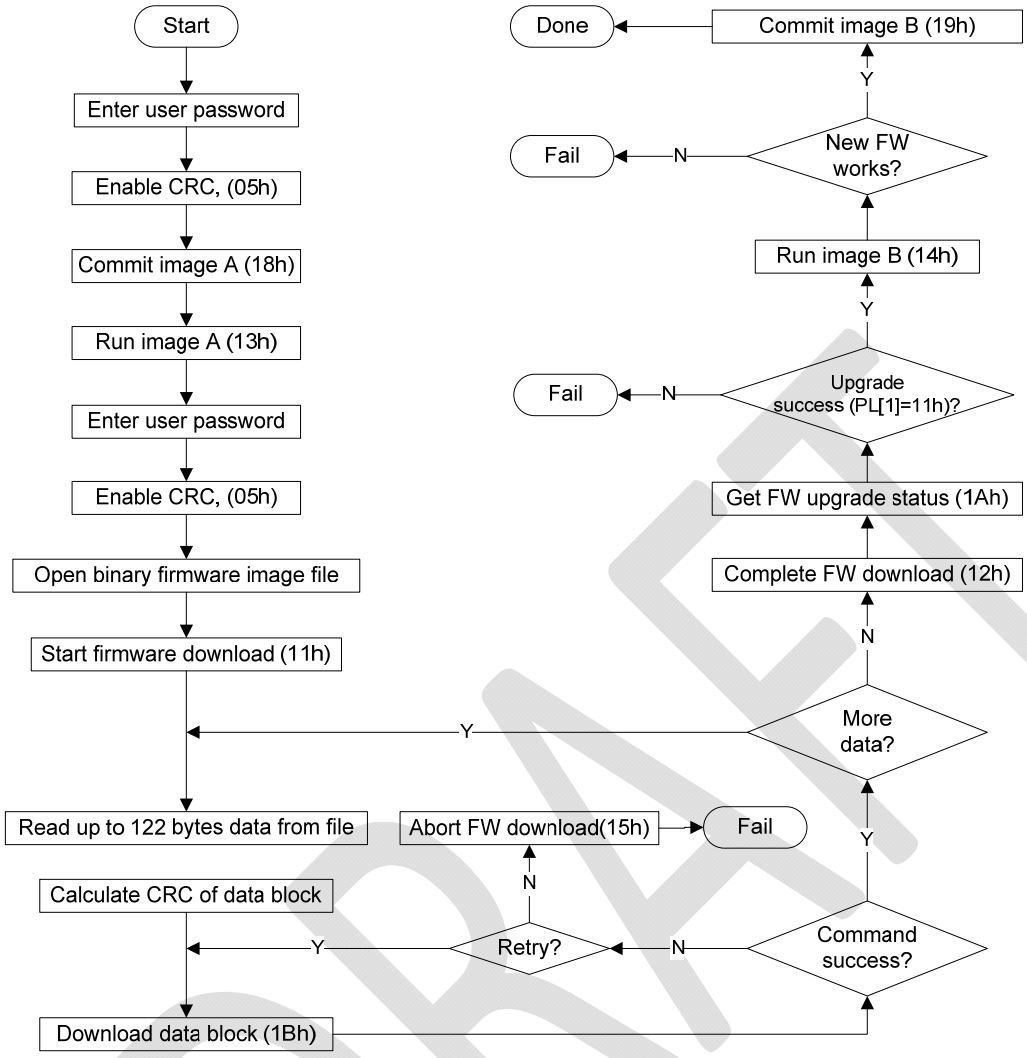
Note all the information contained in the header shall be extracted from the binary image and module vendor shall guarantee the consistency between the header the binary image. For example, the firmware revision number.

For the second part of the firmware upgrade file, ACMIS does not specify the format or the content of firmware binary image. Each module vendor shall compose the firmware image such that it contains all necessary information to interpret, dis-assembly, and execute on the image by a module receives the firmware upgrade. Any secondary firmware, such as a DSP code for a CDR shall be part of the module firmware upgrade image and a module shall be expected to correctly conduct the CDR firmware image upgrade if so intended.

Table 19 Firmware Upgrade Commands

CMD Name	CMD Value	Payload Length	Description
Start Firmware Download	20h	0	Prepare the module to receive firmware upgrade data. Expected STS reply: 50h: Ok to receive FW image, D0h: Not enough NVM space, D1h: Other errors.
Download Image Block	21h	0 - 123	Write a data block to the module for firmware upgrade. The first byte of data of every block (**PL[0]**) should be an image block number (0…255). This block number will roll over to 0 from 255 if more than 256 blocks are transferred. The rest of the payload is the software image, which can contain optional vendor specific descriptors.
Abort Firmware Upgrade	22h	0	Abort firmware upgrade process. Expected STS reply: 50h: Image download aborted. D0h: Command error.
Complete Firmware Download	23h	0	All data has been sent. Module should respond if the firmware upgrade is successful. Expected STS reply: 50h: Full image has been received and image is good. D0h: Image is incomplete. D1h: Image CRC error.
Run Image A	24h	0	Execute the image. Causes firmware to reset. Expected STS reply: D0h: Image A is not valid, execution aborted. D1h: other errors.
Run Image B	25h	0	Execute the image. Causes firmware to reset. Expected STS reply: D0h: Image B is not valid, execution aborted. D1h: other errors.
Commit Image A	26h	0	Commit the new image. Expected STS reply: 50h: Committed successfully. D0h: Command error.
Commit Image B	27h	0	Commit the new image. Expected STS reply: 50h: Committed successfully. D0h: Command error.
Get image status	28h	0	Provides status of currently running and committed image, and status of image A and B. Response from module: **LEN** = 2. Two bytes response. **PL[0]:** Image currently active and committed. Bit 7: Currently active image. 0 = image A; 1 = image B. Bit 6: Committed image. 0 = image A; 1 = image B. Bit 5~0: Reserved. **PL[1]:** Image status. Bit 7~6: Reserved. Bit 5~4: Image A status. 0: No image A' 1: Valid image A present, 2: Image A present is bad. 3: Reserved. Bit 3~2: Reserved. Bit 1~0: Image B status. 0: No image B, 1: Valid image B present, 2: Image B present is bad. 3: Reserved.

Figure 12 Firmware Upgrade Process


Start
Enter user password
Enable CRC, (05h)
Commit image A (18h)
Run image A (13h)
Enter user password
Enable CRC, (05h)
Open binary firmware image file
Start firmware download (11h)
Read up to 122 bytes data from file
Calculate CRC of data block
Download data block (1Bh)
Retry?
Y
N
Abort FW download(15h)
Fail
Command success?
More data?
Complete FW download (12h)
Get FW upgrade status (1Ah)
Upgrade success (PL[1]=11h)?
Run image B (14h)
New FW works?
Commit image B (19h)
Done

5 MODULE MEMORY MAP

This subsection defines the Memory Map for an ACMIS Module used for serial ID, module function and feature advertisement, digital diagnostics, optical monitoring and control functions. The interface is mandatory for all ACMIS devices. The memory map has been designed to accommodate 8 or more electrical lanes. Single TWI address A0h and paging mechanism are used.

Figure 13 CMIS/ACMIS Memory Map depicts the structure of the memory map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure supports a flat 256-byte memory for passive copper cables and permits timely access to addresses in the lower page, e.g. Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function.

The structure also provides address expansion by adding additional upper pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space. The lower page and upper page 00 are required for passive copper cables and are always implemented. In addition, upper pages 1, 2 and bank 0 pages 10h and 11h are required for active modules.

Bank pages are provided to provide the ability to support modules with more than 8 lanes. Bank 0 provides lane-specific registers for the lower 8 lanes. Each additional bank provides support for an additional 8 lanes. Reserved bytes are for future use and shall be write as “don’t care” and read as 0.

Other organizations shall contact the managing organization or the editor of this document to request allocations of registers. The use of custom bytes is not restricted and may be vendor defined. The use of registers defined as custom may be subject to additional agreements between module users and vendors.

5.1 Module memory map overview

Figure 13 CMIS/ACMIS Memory Map

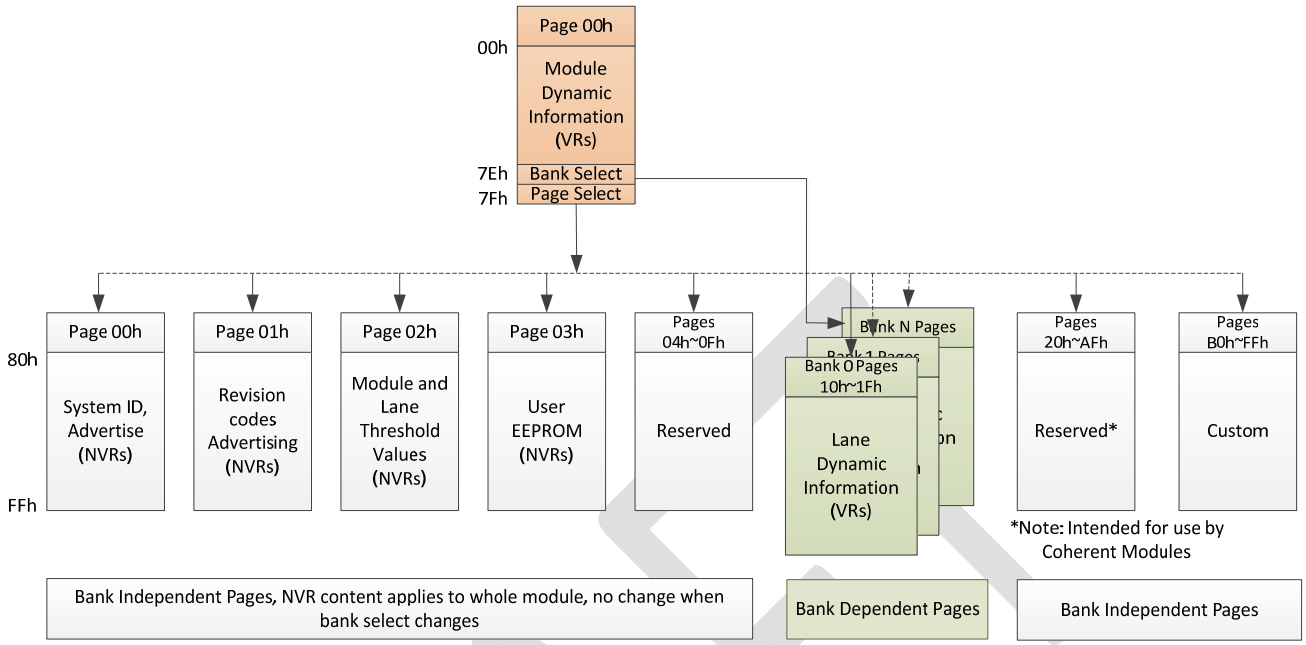
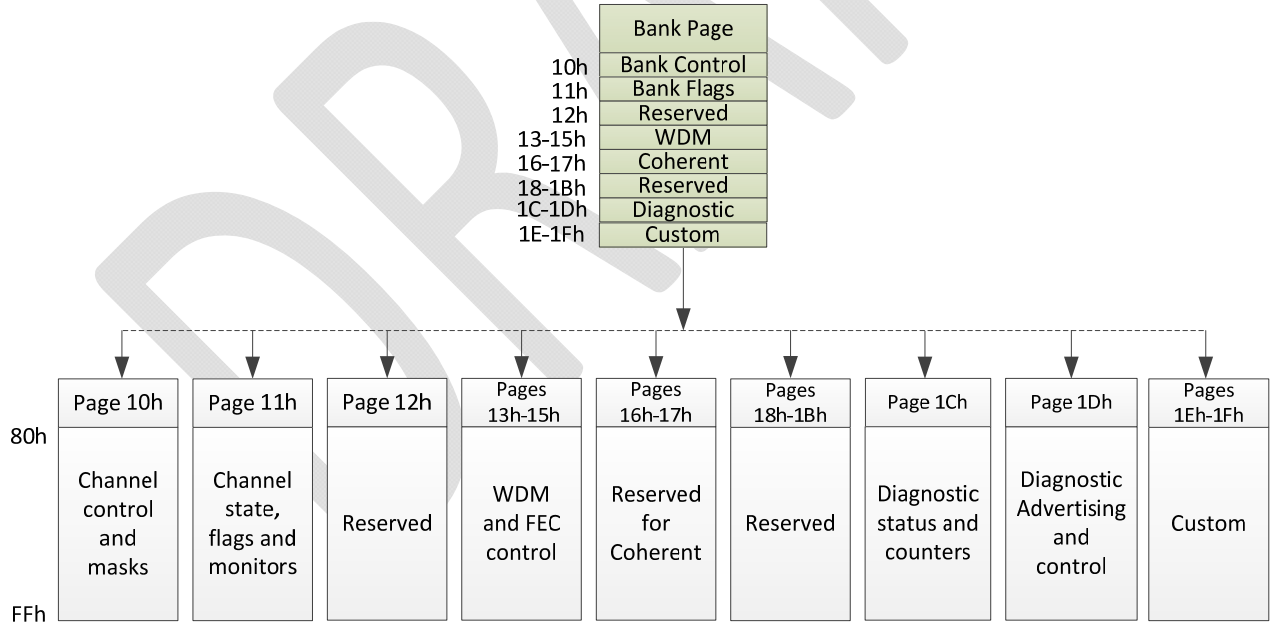


Figure 14 CMIS Memory Map Banked Pages



5.2 Lower Page Memory Map

1

Table 20 Lower Page Memory Map

Lower Page						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
Base ID Information						
0	1	RO	7~0	Module_Identifier	Module ID defined by SFF-8024	N/A
1	1	RO	7~0	Version ID	MIS Version ID. The upper nibble is the whole number part and the lower nibble is the decimal part. Example: 01h indicates version 0.1, 21h indicates version 2.1.	N/A
2	1	RO	7	Flat_mem	Upper memory flat or paged. Upper memory addressing is flat or paged. 0b: Paged memory with multiple pages 1b: Flat memory (only page 00h implemented)	
			6	CLEI present	CLEI code present in upper page 00h	
			5~4	MIS Type	Two-bit field indicates what MIS is used, Version ID at byte 01 is extended to indicate MIS version number for all the types below. 00h: CMIS, 01h: ACMIS, 10h: SFF-8636, 11h: Other types.	
			3-2	TWI Maximum speed	Indicates maximum two-wire serial speed supported by module 00b=Module supports up to 400 kHz 01b=Module supports up to 1 MHz 10b=Reserved 11b=Reserved	
			1~0	Reserved		
3	1	RO	7-4	Reserved		
			3-1	Module state	Current state of Module 000b: Reserved, 001b: ModuleLowPwr, 010b: ModulePwrUP, 011b: MoudleReady, 100b: MoudlePwrDn, 101b: Fault, 110b~111b: Reserved.	
			0	Interrupt	Digital state of Interrupt output signal 0b=Interrupt asserted 1b=Interrupt not asserted (default)	
4	1	RO	7~0	Bank 0 lane flag summary	Summary bit for all flags in each lane. Bit 7 is summary of lane 8, Bit 0 is summary of lane 1. 4 Banks are supported. 1b: One or more of the flag bits in a lane is set for bank 0.	RQD
5	1	RO	7~0	Bank 1 lane flag summary		RQD
6	1	RO	7~0	Bank 2 lane flag summary		RQD
7	1	RO	7~0	Bank 3 lane flag summary		RQD
8	1	RO	7-1	Reserved		RQD
			0	L-Module state changed flag	Latched Indication of change of Module state	RQD
9	1	RO	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	Opt.
			6	L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag	
			5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
			4	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag	
			3	L-Temp Low Warning	Latched low temperature warning flag	
			2	L-Temp High Warning	Latched high temperature warning flag	
			1	L-Temp Low Alarm	Latched low temperature alarm flag	
			0	L-Temp High Alarm	Latched high temperature alarm flag	
10	1	RO	7	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor	
			6	L-Aux 2 High Warning	Latched high warning for Aux 2 monitor	
			5	L-Aux 2 Low Alarm	Latched low alarm for Aux 2 monitor	
			4	L-Aux 2 High Alarm	Latched high alarm for Aux 2 monitor	
			3	L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor	
			2	L-Aux 1 High Warning	Latched high warning for Aux 1 monitor	
			1	L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor	
			0	L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor	
11	1	RO	7	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor	Opt.
			6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor	

Lower Page						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
			5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor	
			4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor	
			3	L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor	
			2	L-Aux 3 High Warning	Latched high warning for Aux 3 monitor	
			1	L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor	
			0	L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor	
12	1	RO	All	Reserved		
13	1	RO	All	Custom		
14	1	RO	All	Module Monitor 1: Temperature MSB	Internally measured temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	Opt.
15	1	RO	All	Module Monitor 1: Temperature1 LSB		
16	1	RO	All	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage: in 100 µV increments	Opt.
17	1	RO	All	Module Monitor 2: Supply 3.3-volt LSB		
18	1	RO	All	Module Monitor 3: Aux 1 MSB	TEC Current or Reserved monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	Opt.
19	1	RO	All	Module Monitor 3: Aux 1 LSB		
20	1	RO	All	Module Monitor 4: Aux 2 MSB	TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 1/32767% increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments	Opt.
21	1	RO	All	Module Monitor 4: Aux 2 LSB		
22	1	RO	All	Module Monitor 5: Aux 3 MSB	Alternative module case temperature by SFF-8636 definition, or Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2's complement in 1/256 degree Celsius increments. Additional supply voltage monitor: in 100 µV increments. May need Inplemented Monitors Advertisement bits to indicate which option applies. - Editor	Opt.
23	1	RO	All	Module Monitor 5: Aux 3 LSB		
24	1	RO	All	Module Monitor 6: Custom MSB	Custom monitor	Opt.
25	1	RO	All	Module Monitor 6: Custom LSB		
26		RW	7	Reserved		
			6	SW_Only	One-bit control for over-riding the LPMode pin. Not required for DSFP/OSFP module as Low Power pin replacing LPMode pin. 0: LPMode pin controls the power mode of module, 1: LPMode is overridden.	Rqd 0
			5	Squelch control	0b=Tx Squelch reduces OMA 1b=Tx Squelch reduces Pave	Opt.
			4	ForceLowPwr	1b=Forces module into low power mode.	0
			3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=not in reset 1b=Software reset	0
			2-0	Custom		
27~28	2	RO		Reserved		
29	1	RO	All	Reserved		
30	1	RO	All	Custom	Custom Global controls	
31	1	RW	7-1	Reserved		RO
			0	Module State changed flag mask	Masking bit for Module State Changed flag	RQD
32	1	RW	7	M-Vcc3.3 Low Warning flag mask	Masking bit for Vcc3.3 monitor low warning flag	Opt.
			6	M-Vcc3.3 High Warning flag mask	Masking bit for Vcc3.3 monitor high warning flag	
			5	M-Vcc3.3 Low Alarm flag mask	Masking bit for Vcc3.3 monitor low alarm flag	
			4	M-Vcc3.3 High Alarm flag mask	Masking bit for Vcc3.3 monitor high alarm flag	
			3	M-Temp Low Warning flag mask	Masking bit for temperature monitor low warning flag	

Lower Page						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
			2	M-Temp High Warning flag mask	Masking bit for temperature monitor high warning flag	
			1	M-Temp Low Alarm flag mask	Masking bit for temperature monitor low alarm flag	
			0	M-Temp High Alarm flag mask	Masking bit for temperature monitor high alarm flag	
33	1	RW	7	M-Aux 2 Low Warning flag mask	Masking bit for Aux 2 monitor low warning flag	Opt.
			6	M-Aux 2 High Warning flag mask	Masking bit for Aux 2 monitor high warning flag	
			5	M-Aux 2 Low Alarm flag mask	Masking bit for Aux 2 monitor low alarm flag	
			4	M-Aux 2 High Alarm flag mask	Masking bit for Aux 2 monitor high alarm flag	
			3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
			2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
			1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
			0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
34	1	RW	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	Opt.
			6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
			5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
			4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
			3	M-Aux 3 Low Warning flag mask	Masking bit for Aux 3 monitor low warning flag	
			2	M-Aux 3 High Warning flag mask	Masking bit for Aux 3 monitor high warning flag	
			1	M-Aux 3 Low Alarm flag mask	Masking bit for Aux 3 monitor low alarm flag	
			0	M-Aux 3 High Alarm flag mask	Masking bit for Aux 3 monitor high alarm flag	
35	1	RW	All	Reserved flag mask		
36	1	RO	All	Custom	Module level flag masks	
37	1	RO		Reserved		00
38	1	RO		Reserved		
39~62	25	RO		Reserved		
63	1	RW		Boot Record Manager	This byte manages the data flow between host, Control Register Set and Module Boot Record. It consists of a 3-bit command field and a 5-bit Boot Record Number. The Commands manage Control Set restore, save, apply immediately, and assign next power on reset default. The MBR Number points a saved MBR.	
			7~5	MBR Command	3-bit code for Module Boot Record management.	000b
					Code: Command Description	
					000b: Enable updating hardware with the content of Control Set Registers. Any write to Control Set Register shall take effect immediately. MBR Number has no effect.	
					001b: Disable updating hardware with the content of Control Set Registers. Control Set Registers are in editing mode. MBR Number has no effect.	
					010b: Load Module Boot Record content to Control Set Registers. If Control Set Register update is enabled the content shall take effect immediately. If disabled, no effect with loaded content. Control Set Number is the MBR number.	
					011b: Save the content of Control Set Registers to a MBR pointed by MBR number.	
					100b: Assign a MBR pointed by MBR number as the next time power-on default.	
					101b ~111b: Reserved.	
			4~0	MBR Number	MBR Number - 5-bit field to point to a Module Boot Record. On power-up this field contains the default MBR number. 0: ~15: ACMIS MBR numbers, 16~31: Custom MBR (User defined) numbers.	0000 0b
64~84	21	RO		Custom		

Lower Page						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
85	1	RO	7~0	Module Type Advertising Code	This is defined in CMIS 3.0. The actual meaning is Module Media Type.	Rqd.
86~117	32	RO	7~0	Reserved	Originally used by CMIS for App Code advertisement. Still can be used as App Code advertisement for backward compatibility especially for passive cable applications	
118~121	4	WO	7~0	Password Change	Write a new password in Bytes 118-121 when the correct current module manufacturer password has been entered in Bytes 122-125, with the high order bit being ignored and forced to a value of 0 in the new password. The password entry field shall be set to 00000000h on power up and reset.	
122~125	4	WO	7~0	Password Entry	The Password entry bytes shall be write only and be used to control write access to the custom page 03h (EEPROM) and other custom upper pages. Additionally, module vendors may use this function to implement write protection of Serial ID and other read only information. Note that multiple module manufacturer passwords may be defined to allow selective access to write to various sections of memory. Password shall not be required to read lower Page 00h or Upper Page 00h, 01h, 02h, 03h, 10h or 11h. Host manufacturer and module manufacturer passwords shall be distinguished by the high order bit (bit 7, Byte 122). All host manufacturer passwords shall fall in the range of 00000000h to 7FFFFFFFh, and all module manufacturer passwords in the range of 80000000h to FFFFFFFFh. Host system manufacturer passwords shall be initially set to 00001011h in new modules.	
126	1	RW	7~0	Bank Select	8-bit unsigned integer to select a memory page bank.	
127	1	RW	7~0	Page Select	8-bit unsigned integer to select an upper page.	

5.3 Upper Pages

Note most of the content of memory maps will be copied over from CMIS with some formatting. New functions will be added with new registers. Some complex function registers will be commented as “Not required”.

5.3.1 Upper Page 00h Static Read-only Module Identification Information

This page remains synchronized with CMIS except the following registers.

Table 21 U00h (0) Module Identification Information

Upper Page 00h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
Basic Module ID information						
128	1	RO	7~0	Identifier	Module Identifier Number defined by SFF8024 N1: DSFP, TBD N2: OSFP, TBD …	Rqd.
129~144	16	RO	7~0	Vendor Name	16-byte field containing characters in ASCII, left aligned, padded on the right with ASCII spaces (20h). All ASCII fields bellow use same aligning and padding rules.	Rqd.
145~147	3	RO	7~0	Vendor Org Unique Identifier	3-byte vendor OUI of IEEE Company Identifier for the vendor. A value of all 0 indicates vendor OUI unspecified.	Rqd.
148~163	16	RO	7~0	Vendor Part Number	16-byte ASCII vendor part number (PN). All zero field indicates vendor PN unspecified.	Rqd.
164~165	2	RO	7~0	Vendor Revision Number	2-byte field containing ASCII characters defining vendor’s product revision number. Value all zero indicates that vendor Rev unspecified.	Rqd.
166~181	16	RO	7~0	Vendor Serial Number	16-byte field containing ASCII characters defining vendor’s product serial number (SN), all zero indicates SN unspecified.	Rqd.
182~183	2	RO	7~0	Date Code of Year	ASCII code, two low order digits of year e.g., 00 = 2000.	Rqd.

Upper Page 00h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
184~185	2	RO	7~0	Date Code of Month	ASCII code, two digits for month (01= Jan., …, 12=Dec.)	Rqd.
186~186	2	RO	7~0	Date Code of Day	ASCII code, two digits for day of month (01~31)	Rqd.
188~189	2	RO	7~0	Lot Code	ASCII code, custom lot code, may be blank	Opt.
190~209	10	RO	7~0	CLEI Code	ASCII code, 10-digit containing vendor's CLEI code.	Opt.
200	1	RO	7~5	Module Card Power Class	3-bit code for Power Class Value, See respective hardware spec.	Rqd.
			4~0	Reserved		
201	1	RO	7~0	Max Power	Maximum power consumption in multiples of 0.25 W rounded up to the next whole multiple of 0.25 W.	Rqd.
202	1	RO	7~6	Length multiplier (Copper or active cable)	2-bit code of multiplier for value in bits 5~0. 00b = 0.1, 01b = 1, 10b = 10, 11b = 100.	Rqd.
			5~0	Base Length of Copper or Active Cable	6-bit unsigned integer representing the base value in meters. This value is further multiplied by Length Multiplier (Bits 7~6 above).	Rqd.
203	1	RO	7~0	Connector Type	Type of connector present in the module. See SFF-8024 Table 4-3 for codes.	Rqd.
204	1	RO	7~0	5 GHz Attenuation	Passive copper cable attenuation at 5 GHz in 1 dB increments	Opt.
205	1	RO	7~0	7 GHz Attenuation	Passive copper cable attenuation at 7 GHz in 1 dB increments	Opt.
206	1	RO	7~0	12.9 GHz Attenuation	Passive copper cable attenuation at 12.9 GHz in 1 dB increments	Opt.
207	1	RO	7~0	25.8 GHz Attenuation	Passive copper cable attenuation at 25.8 GHz in 1 dB increments	Opt.
206~207	3			Reserved		
210	1	RO	7~0	Near End Implementation of Media Lane N	8-bit field indicate if a media lane is implemented at near end. N = 1, …, 8 corresponding to bits 7~0. With optical modules a media lane may be a fiber or a wavelength.	Opt.
211	1	RO	7~5	Reserved		
			4~0	Far End Configuration	See Table 35 in CMIS for details	Opt.
212	1	RO	7~0	Media Interface Technology	8-bit unsigned integer as the description of physical device of media. 00h: 850 nm VCSEL, 01h: 1310 nm VCSEL, 02h: 1550 nm VCSEL, 03h: 1310 nm FP, 04h: 1310 nm DFB, 05h: 1550 nm DFB, 06h: 1310 nm EML, 07h: 1550 nm EML, 08h: Others, 09h: 1490 nm DFB, 0Ah: Copper cable un-equalized, 0Bh: Copper cable passive equalized, 0Ch: Copper cable, near and far end limiting active equalizers, 0Dh: Copper cable, far end limiting active equalizers, 0Eh: Copper cable, near end limiting active equalizers 0Fh: Copper cable, linear active equalizers, 10h~FFh: Reserved	Rqd.
213~220	8	RO		Reserved		0
221	1	RO		Custom		
222	1	RO		Checksum	Checksum shall be the low order 8 bits of the sum of the contents of all the bytes from 128 to 221, inclusive.	Rqd.
223~255	33	RO		Custom Info NV	Content defined custom, not by MSA or ACMIS.	Opt.

5.3.2 Upper Page 01h Module Capability Advertisement-

Table 22 U01h (1) Module Capability Advertisement

Upper Page 01h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
Basic ID Information						
128	1	RO	7~0	Firmware A Major Revision Number	8-bit unsigned integer for module firmware A major revision number. See U01.174~175 for Image B rev number.	Rqd.
129	1	RO	7~0	Firmware A Minor Revision Number	8-bit unsigned integer for module firmware A minor revision number. See U01.174~175 for Image B rev number.	Rqd.
130	1	RO	7~0	Hardware Major Revision Number	8-bit unsigned integer for module hardware major revision number	Rqd.
131	1	RO	7~0	Hardware Minor Revision Number	8-bit unsigned integer for module hardware minor revision number	Rqd.
132	1	RO		Maximum Length for SMF Fiber	This byte and next 4 bytes are 8-bit unsigned integer representing maximum fiber media length for each type of fiber media at the maximum bit rate. Active optical cables shall populate with 0 and instead report in byte 220.	Rqd.
			7-6	Length multiplier(SMF)	Link length multiplier for SMF fiber (Supported length see SFF 8074i). 00 = 0.1 (1 to 6.3 km) 01 = 1 (1 to 63 km) 10, 11 = reserved	Rqd.
			5-0	Base Length (SMF)	Base link length for SMF fiber. Must be multiplied by value in bit	Rqd.
133	1	RO	7-0	Maximum Length (OM5)	Link length supported for OM5 fiber, units of 2m (2 to 510 m)	Rqd.
134	1	RO	7-0	Length (OM4)	Link length supported for OM4 fiber, units of 2m (2 to 510 m)	Rqd.
135	1	RO	7-0	Length (OM3)	Link length supported for EBW 50/125 µm fiber (OM3), units of 2m (2 to 510 m)	Rqd.
136	1	RO	7-0	Length (OM2)	Link length supported for 50/125 µm fiber (OM2), units of 1m (1 to 255 m)	Rqd.
137	1	RO		Reserved		Rqd.
138~139	2	RO	7~0	Wavelength	2-byte 16-bit unsigned integer with byte order big endian representing nominal transmitter output wavelength at room temperature. Bit resolution is 0.05 nm. (single Tx case. For multi-wavelength module see end of U11h, media lane to wavelength mapping)	Rqd.
140~141	2	RO	7~0	Wavelength Tolerance	2-byte 16-bit unsigned integer with byte order in big endian representing worst case +/- range of the transmitter output wavelength under all normal operating conditions. Bit resolution is 0.005 nm.	Rqd.
142	1	RO	7-6	Reserved	RORQD	
		RO	5	Diagnostic pages implemented	Bank page 1Ch-1Dh implemented for diagnostic features	
			4~3	Reserved		
			2	Page 03h implemented	Indicates User page 03h implemented	
			1-0	Implemented Banks	Indicates bank pages implemented for pages 10h-1Fh 00b=bank 0 implemented 01b=banks 0 and 1 implemented 10b, 11b=reserved	
143	1	RO	7-5	ModSelL wait time exponent	The ModSelL wait time value is the mantissa x 2^exponent expressed in micro-seconds. In other words, the mantissa field is shifted up by the number of bits indicated in the exponent field (time = mantissa << exponent)	NR for ACMIS
			4~0	ModSelL Wait Time Mantissa		
144	1	RO	7-4	ModulePwrDn_MaxDuration	Encoded maximum duration of Module Power Down state, see Table 23 State Duration Encoding (Page 01h). Host shall not wait longer than this duration.	RQD
			3-0	ModulePwrUp MaxDuration	Encoded maximum duration of module power up state, see Table 23 State Duration Encoding (Page 01h). Host shall not wait longer than this duration.	RQD
145	1	RO	7	Cooling implemented	0b=Uncooled transmitter device 1b=Cooled transmitter	RQD
			6-5	Tx input clock recovery capabilities	00b=module requires all Tx input lanes to be in a single Tx synchronous group	RQD

Upper Page 01h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
					01b=module allows Tx input lanes 1-4 and 5-8 to be in separate Tx synchronous groups 10b=module allows Tx input lanes 1-2, 3-4, 5-6, 7-8 to be in separate Tx synchronous groups 11b=module allows each Tx input lane to be in a separate Tx synchronous group	
			4-3	Reserved	RO	
			2	Aux 3 Monitor type	1b=Aux 3 monitor is Vcc2 0b=Aux 3 monitor is Laser Temperature	Opt.
			1	Aux 2 Monitor type	1b=Aux 2 monitor is TEC current 0b=Aux 2 monitor is Laser Temperature	Opt.
			0	Aux 1 Monitor type	1b=Aux 1 monitor is TEC current 0b=Aux 1 monitor is reserved	Opt.
146	1	RO	7-0	Maximum module temperature	Maximum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	Opt.
147	1	RO	7-0	Minimum module temperature	Minimum allowed module case temperature 8-bit signed 2's complement value in 1 deg C increments. A value of all zeroes indicates not specified.	Opt.
148	1	RO	7-0	Propagation Delay MSB	Propagation delay of the non-separable AOC in multiples of 10 ns rounded to the nearest 10 ns. A value of all zeroes indicates not specified.	Opt.
149	1	RO	7-0	Propagation Delay LSB		
150	1	RO	7-0	Minimum operating voltage	Minimum supported module operating voltage, in 20 mV increments (0 - 5.1 V) A value of all zeroes indicates not specified.	Opt.
151	1	RO	7	Detector type	0b=PIN detector 1b=APD detector	RQD
			6-5	RX Output Eq type	00b=Peak-to-peak amplitude stays constant, or not implemented, or no information 01b=Steady-state amplitude stays constant 10b=Average of peak-to-peak and steady-state amplitude stays constant 11b=Reserved	
			4	Rx Optical Power Measurement type	0b=OMA 1b=average power	
			3	Rx LOS type	0b=Rx LOS responds to OMA 1b=Rx LOS responds to Pave	
			2	Rx LOS fast mode implemented	0b=Rx LOS fast mode not implemented 1b=Rx LOS fast mode implemented Refer to form factor hardware specification for timing requirements	
			1	Tx Disable fast mode implemented	0b=Tx Disable fast mode not implemented 1b=Tx Disable fast mode implemented Refer to form factor hardware specification for timing requirements	
			0	Module-Wide Tx Disable	0b=Tx Disable implemented per lane 1b=Any Tx Disable control bit being set disables	
152	1	RO	7-0	Per lane CDR Power saved	Minimum power consumption saved per CDR per lane when placed in CDR bypass in multiples of 0.01 W rounded to up to the next whole multiple of 0.01 W	
153	1	RO	7	Rx Output Amplitude code 0011b implemented1	0b=Amplitude code 0011b not implemented 1b=Amplitude code 0011b implemented	Opt.
			6	Rx Output Amplitude code 0010b implemented1	0b=Amplitude code 0010b not implemented 1b=Amplitude code 0010b implemented	
			5	Rx Output Amplitude code 0001b implemented1	0b=Amplitude code 0001b not implemented 1b=Amplitude code 0001b implemented	
			4	Rx Output Amplitude code 0000b implemented1	0b=Amplitude code 0000b not implemented 1b=Amplitude code 0000b implemented	
			3-0	Max Tx Input Eq	Maximum supported value of the Tx Input Equalization control for manual/fixed	
154	1	RO	7-4	Max Rx Output Eq Post-cursor	Maximum supported value of the Rx Output Eq Post-cursor control. (see Table 13)	Opt.
			3-0	Max Rx Output Eq Pre-cursor	Maximum supported value of the Rx Output Eq Pre-cursor control (see Table 13)	
Implemented Controls Advertisement						
155	1	RO	7	Wavelength control implemented	0b=No wavelength control	RQD

Upper Page 01h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
					1b=Active wavelength control implemented	
			6	Tunable transmitter implemented	0b=Transmitter not tunable 1b=Transmitter tunable	
			5-4	Tx Squelch implemented	00b=Tx Squelch not implemented 01b=Tx Squelch reduces OMA 10b=Tx Squelch reduces Pave 11b=User control, both OMA and Pave squelch supported. (see Table 23)	
			3	Tx Force Squelch implemented	0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented	
			2	Tx Squelch Disable implemented	0b=Tx Squelch Disable not implemented 1b=Tx Squelch Disable implemented	
			1	Tx Disable implemented	0b=Tx Disable not implemented 1b=Tx Disable implemented	
			0	Tx Polarity Flip implemented	0b=Tx Polarity Flip not implemented	
156	1	RO	7-3	Reserved	RORQD	
			2	Rx Squelch Disable implemented	0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented	RQD
			1	Rx Disable implemented	0b=Rx Disable not implemented 1b=Rx Disable implemented	
			0	Rx Polarity Flip implemented	0b=Rx Polarity Flip not implemented	
157	1	RO	7-4	Reserved	RO RQD	
			3	Tx Adaptive Input Eq Fault flag implemented	0b=Tx Adaptive Input Eq Fault flag not implemented 1b=Tx Adaptive Input Eq Fault flag implemented	RQD
			2	Tx CDR LOL flag implemented	0b=Tx CDR Loss of Lock flag not implemented 1b=Tx CDR Loss of Lock flag implemented	
			1	Tx LOS flag implemented	0b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented	
			0	Tx Fault flag implemented	0b=Tx Fault flag not implemented 1b=Tx Fault flag implemented	
158		RO	7-3	Reserved		
			2	Rx LOL flag implemented	0b=Rx CDR Loss of Lock flag not implemented 1b=Rx CDR Loss of Lock flag implemented	RQD
			1	Rx LOS flag implemented	0b=Rx Loss of Signal flag not implemented 1b=Rx Loss of Signal flag implemented	
			0	Reserved		
Implemented Monitors Advertisement						
159	1	RO	7-6	Reserved	RO RQD	
			5	Custom monitor implemented	0b=Custom monitor not implemented 1b=Custom monitor implemented	RQD
			4	Aux 3 monitor implemented	0b=Aux 3 monitor not implemented 1b=Aux 3 monitor implemented	
			3	Aux 2 monitor implemented	0b=Aux 2 monitor not implemented 1b=Aux 2 monitor implemented	
			2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented 1b=Aux 1 monitor implemented	
			1	Internal 3.3 Volts monitor implemented	0b=Internal 3.3 V monitor not implemented 1b=Internal 3.3 V monitor implemented	
			0	Temperature monitor implemented	0b=Temperature monitor not implemented	
160	1	RO	7~6	Reserved.		
			4-3	Tx Bias current measurement and threshold multiplier	Multiplier for 2uA Bias current increment used in Tx Bias current monitor and threshold registers (see Table 51 and Table 70) 00b=multiply x1 01b=multiply x2 10b=multiply x4 11b= reserved.	
			2	Rx Optical Input Power monitor implemented	0b=Rx Optical Input Power monitor not implemented 1b=Rx Optical Input Power monitor implemented	

Upper Page 01h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
			1	Tx Output Optical Power monitor implemented	0b=Tx Output Optical Power monitor not implemented 1b=Tx Output Optical Power monitor implemented	
			0	Tx Bias monitor implemented	0b=Tx Bias monitor not implemented 1b=Tx Bias monitor implemented	
161	1	RO	7	Reserved	RO RQD	
			6~5	Reserved		
			4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented 1b=Tx Input Eq Freeze implemented	
			3	Adaptive Tx Input Eq implemented	0b=Adaptive Tx Input Eq not implemented 1b=Adaptive Tx Input Eq implemented	
			2	Tx Input Eq fixed manual control implemented	0b=Tx Input Eq Fixed Manual control not implemented 1b=Tx Input Eq Fixed Manual control implemented	
			1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Tx CDR Bypass control implemented	
			0	Tx CDR implemented	0b=Tx CDR not implemented 1b=Tx CDR implemented	
162	1	RO	7-6	Reserved		
			5	Reserved		
			4-3	Rx Output Eq control implemented	00b=Rx Output Eq control not implemented 01b=Rx Output Eq Pre-cursor control implemented 10b=Rx Output Eq Post-cursor control implemented 11b=Rx Output Eq Pre- and Post-cursor control implemented	
			2	Rx Output Amplitude control implemented	0b=Rx Output Amplitude control not implemented 1b=Rx Output Amplitude control implemented	
			1	Rx CDR Bypass control implemented	0b=Rx CDR Bypass control not implemented (if CDR is implemented, it will be enabled) 1b=Rx CDR Bypass control implemented	
			0	Rx CDR implemented	0b=Rx CDR not implemented 1b=Rx CDR implemented	
Lane Mapping Registers						
163	1	RO	7~0	PMD Type and Lane Map Code	8-bit integer code the module PMD type and the lane map. Reference Appendix A for encoding of each form factor.	Rqd.
164	1	RO	7~0	Host Lane Map	Bits 7~0 represent presence of each host lane in a bank. 0b: No host lane present, 1b: Host lane present. Example: 11000000b indicates a 2-host lane module. This byte and next byte also indicate how host lanes map into media lanes.	Rqd.
165				Media Lane Map	Bits 7~0 represent presence of each media lane in a bank. 0b: No media lane present, 1b: Media lane present. Example: 11000000b indicates a 2-media lane module.	Rqd.
166	1	RO	7~5	Inter-lane Clock Dependency	3-bit code to indicate reference clock dependency between lanes. 000b: Lane to lane independent, 001b: Clock synchronized for every 2 lanes, 010b: Clock synchronized for every 4 lanes, 011b: Clock synchronized for every 8 lanes, 100b~111b: reserved.	
			4~0	Reserved		
167~173	9	RO		Reserved	On reserve in CMIS 3.0 (163~175)	
174	1	RO	7~0	Module firmware B major revision	Numeric representation of module firmware image B major revision number	Opt
175	1	RO	7~0	Module firmware B minor revision	Numeric representation of module firmware image B minor revision number	Opt
176~190	15	RO		Reserved	On reserve in CMIS 3.0	
191~222	32	RO		Custom	Same as in CMIS 3.0	

Upper Page 01h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
223~250	28	RO	7~0	Reserved	Was used for Extended Module Host-Media Interface Adv. Options.	
251~254	4	RO	7~0	Reserved	Same as in CMIS 3.0	
255	1	RO	7~0	Checksum	Checksum of bytes 130~254. Firmware version bytes 128, 129 and 174, 175 are excluded from the checksum to allow module implementers programmatically generate these fields and avoid requiring a memory update when firmware is updated.	

Table 23 State Duration Encoding (Page 01h)

ENCODING	MAXIMUM STATE DURATION
0000b	Maximum state duration is less than 1 ms
0001b	1 ms <= maximum state duration < 5 ms
0010b	5 ms <= maximum state duration < 10 ms
0011b	10 ms <= maximum state duration < 50 ms
0100b	50 ms <= maximum state duration < 100 ms
0101b	100 ms <= maximum state duration < 500 ms
0110b	500 ms <= maximum state duration < 1 s
0111b	1 s <= maximum state duration < 5 s
1000b	5 s <= maximum state duration < 10 s
1001b	10 s <= maximum state duration < 1 min
1010b	1 min <= maximum state duration < 5 min
1011b	5 min <= maximum state duration < 10 min
1100b	10 min <= maximum state duration < 50 min
1101b	Maximum state duration >= 50 min
1110b	Reserved
1111b	Reserved

5.3.3 Upper Page 02h Thresholds for Alarms and Warnings

This page is identical to CMIS.

Table 24 U02h Overview

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Customizable space	
255	1	Checksum	Covers bytes 128-254

5.3.4 Upper Page 03h (3) User EEPROM

User EEPROM, optional.

Table 25 U03h (3) User EEPROM

Upper Page 03h User EEPROM						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	*Init*
128	127	RO	7~0	EEPROM Content	User defined content	
255	1	RO	All	Check Sum	Check sum of this whole page excluding byte 255.	N/A

5.3.5 Upper Page 04h (4) ACMIS Advertisement Page

Table 26 U04h (4) ACMIS Application Selection Advertisement

Upper Page 04h Application Selection Code Advertisement (ACMIS only)						
Byte	***Size***	***Access***	***Bit***	***Byte or Bit Field Name***	***Description***	***Init***
Application Selection Advertisement (Maximum 31 codes allowed)						
128	1	RO	7~0	Number of Application Selection Supported	Bits 7~5 are reserved. Bits 4~0: a 5-bit unsigned integer represents the number of Application Selection this module supports.	
129	1	RO		Module Media Type (Module Type Encoding 85 in CMIS, also seems overlapping with U00h:212)	8-bit unsigned value to advertise module media type. 00h: Undefined, 01h: Optical Interfaces MMF (Appendix A), 02h: Optical Interfaces SMF (Appendix A), 03h: Passive Copper Cable (Appendix A), 04h: Active Cables (Appendix A), 05h: BASE-T (Appendix A), 06h~3Fh: reserved, 40h~8Fh: Custom, 90h~FFh: Reserved.	
130~131	2	RO	7~0	Application Selection 1	This 2-byte data structure contains Application Selection 0. The first byte is (at smaller byte address) Module Host Interface Code and the second byte is Module Media Interface Code, both extracted from Code Books in Appendix B. Use byte 129 Module Media Type to determine which media code book to use for the Module Media Interface Code.	
132~193	62	RO	7~0	Application Selection 2 to 32	These bytes are allocated for the rest of total 31 Two-byte Application Selections 1 to 31. Each two-byte data has exactly the same definition of Application Selection 0. Note each module may support up to 32 Application Selections. If less 32, all the supported Application Selections are required to continuously occupy the list. Un-used bytes shall be set to 0.	N/A
194~254	61	RO	All	Reserved	May be used for extension of Application Selection codes.	
255	1	RO	All	Check Sum	Check sum of this whole page excluding byte 255.	N/A

5.3.6 Upper Page 0Fh (15) Command and Data Block

Table 27 U9Fh (15) Command and Data Block

ADDR	SIZE	ACCESS TYPE	BIT	REGISTER NAME BIT FIELD NAME	DESCRIPTION	DEFAULT VALUE
128	1	RO	7~0	STS	CDB status and error message of last command CMD execution.	00h
129	1	RW	7~0	CMD	Command byte, see command table for details.	00h
130	1	RW	7~0	LEN	Payload size N in bytes.	00h
131	2	RW	7~0	CRC	CRC-16 checksum for registers CMD, LEN, and PL.	00h
133	N	RW	7~0	PL	Payload data of size N, N_{max} = 123. Payload are parameters of either host command or module response.	00h

5.3.7 Upper Page 10h (16) Lane Control and Flag Registers

Table 28 U10h (16) Lane Control and Flag Registers

Upper Page 10h (whole page is part of Module Control Register Set)						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
128	1	RW	All	Host Lane Power Control	Bitwise control over each host lane. 0b: Turn corresponding host lane off, 1b: Turn corresponding host lane on.	
TX General Controls (outside of Staged Control Set 0/1)						
129	1	RW	All	TX Polarity Flip	Per bit per lane. 0b: No polarity flip, 1b: Tx input polarity flip.	
130	1	RW	All	TX Disable	0b: Tx output enabled for medial lane, 1b: Tx output disabled for medial lane.	
131	1	RW	All	TX Squelch Disable	0b: Tx output squelch permitted for a lane, 1b: Tx output squelch not permitted for a lane.	
132	1	RW	All	Tx Force Squelch	Per bit per lane. Bit 7 = Lane 8, Bit 0 = Lane 1. 0b: No impact Tx behavior for media lane, 1b: Tx output squelched for media lane.	
133	1	RW	All	Media Lane Power Control	Bitwise control over each media lane. 0b: Turn corresponding media lane off, 1b: Turn corresponding media lane on.	
134	1	RW	All	Tx Input Eq. Adaptation Freeze	Bit-lane wise control on Tx Input Eq (ACTLE) adaptation. 0b: Tx Input eq. (ACTLE) adaptation active, 1b: Tx Input eq. (ACTLE) adaptation frozen at last value.	
~~135~~	~~1~~	~~RW~~	~~All~~	~~TX Input Eq Adaptation Store~~ Reserved now	~~Two bit a lane, 7~6 for TX4, … 1~0 for TX1,.~~	
~~136~~	~~1~~	~~RW~~	~~All~~	~~TX Input Eq Adaptation Store~~ Reserved now	~~Two bit a lane, 7~6 for TX8, … 1~0 for TX5,.~~	
RX General Controls (Outside of Staged Control Set 0/1)						
137	1	RW	All	Rx Polarity Flip		
138	1	RW	All	Rx Output Disable		
139	1	RW	All	Rx Squelch Disable		
140	1	RW	TBD	Module Control Register Set Lock	To be allocated for locking whole Module Control Register Set. Bit map TBD.	
141~142	2			Reserved		
144~152	8	RO		Reserved for legacy code support		
Control Set Buffer Management Byte						
153~177	25	RO	All	Reserved	Used to be part of Staged Control Set 0, now reserved.	
178~185	8	RW		Application Selection per Lane	Host uses the 8 bytes to program Application Selection for each module lane, both host and media. Once selected, module shall adjust internal parameters to ensure the compliance to each Application Selection. Host and module shall train the equalizer coefficients for best SI.	
			7~5	Reserved		
			4~0	Application Selection Code	5-bit value to select an application Selection Code from Page U04.130~193, totaling 32 App codes. ~~Note that this number is used to store (save) or recall a Staged Control Set in NVR in Control Set Buffer Management byte.~~	
186~193	8	RW	7~4	Tx Input Eq. Control Code	4-bit unsigned value to code manual fixed Eq in dB	
					Code Value / Bit Pattern / Tx Input Eq.	
					0 / 0000 / No Eq.	
					1 ~ 12 / 0001~1100 / 1 ~ 12 dB	
					13~15 / 1101~1111 / Custom	
			3~0	Reserved		
194	1	RW	7~0	Tx Input Adaptive Eq. Enable	Bitwise control, Bit 7 for lane 8, 0 for 1. 0b: Disable (use manual fixed Eq), 1b: Enable (default).	
195	1	RW	7~0	Tx CDR Bypass Control	Bitwise CDR bypass control, Bit 7 for Lane 8, …, 0 for 1.	

<table>
<tr><th colspan="6">Upper Page 10h (whole page is part of Module Control Register Set)</th></tr>
<tr><th>Byte</th><th>Size</th><th>Access</th><th>Bit</th><th>Byte or Bit Field Name</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>0b: CDR bypassed,
1b: CDR engaged.</td></tr>
<tr><td>196~203</td><td>8</td><td>RW</td><td></td><td>Rx Output Eq. Control</td><td>8-byte Rx Output Eq. Control, per byte per lane. 1st byte for 1st lane and so on.</td></tr>
<tr><td></td><td></td><td></td><td>7~4

3~0</td><td>Rx Output Pre-Cursor Eq.

Rx Output Post-Cursor Eq.</td><td>Rx Output Eq. (Emphasis) Codes
Code Value | Bit Pattern | Post-Cursor | Pre-Cursor
0 | 0000 | No Eq. | No Eq.
1 | 0001 | 1 dB | 0.5 dB
2 | 0010 | 2 dB | 1.0 dB
3 | 0011 | 3 dB | 1.5 dB
4 | 0100 | 4 dB | 2.0 dB
5 | 0101 | 5 dB | 2.5 dB
6 | 0110 | 6 dB | 3.0 dB
7 | 0111 | 7 dB | 3.5 dB
8-10 | 1000-1010 | Reserved | Reserved
11-15 | 1011-1111 | Custom | Custom</td></tr>
<tr><td>204~211</td><td>8</td><td>RW</td><td></td><td>Rx Output Amplitude Control</td><td>8-byte Rx Output Amplitude Control. 1st byte for 1st lane, and so on.</td></tr>
<tr><td></td><td></td><td></td><td>7~4</td><td>Rx Output Amplitude Control Code</td><td>Code Value | Bit Pattern | Output Amplitude mVp-p
0 | 0000 | 100-400
1 | 0001 | 300~600
2 | 0010 | 400~800
3 | 0011 | 600~1200
4~14 | 0100~1110 | Reserved
15 | 1111 | Custom</td></tr>
<tr><td></td><td></td><td></td><td>3~0</td><td>Reserved</td><td></td></tr>
<tr><td>212</td><td>1</td><td>RW</td><td>7~0</td><td>Rx CDR Bypass Control</td><td>Bitwise CDR bypass control, Bit 7 for Lane 8, …, 0 for 1.
0b: CDR bypassed,
1b: CDR engaged.</td></tr>
<tr><td colspan="6">Lane Specific Flag Masks (Table 63)</td></tr>
<tr><td>213</td><td>1</td><td>RW</td><td>7~0</td><td>M-Lane n Data Path State Changed flag mask</td><td>1 bit field to mask lane n state change. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>214</td><td>1</td><td>RW</td><td>7~0</td><td>M-TX Media Lane n Fault flag mask</td><td>1-bit field to mask lane n Fault flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>215</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx Lane n LOS flag mask</td><td>1-bit field to mask lane n LOS flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>216</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n CDR LOL flag mask</td><td>1-bit field to mask lane n LOS flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>217</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Adaptive Eq Fault flag mask</td><td>1-bit field to mask lane n Adaptive Eq Fault flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>218</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Power High Alarm flag mask</td><td>1-bit field to mask lane n Tx Power High Alarm flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>219</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Power Low Alarm flag mask</td><td>1-bit field to mask lane n Tx Power High Alarm flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>220</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Power High Warning flag mask</td><td>1-bit field to mask lane n Tx Power High Warning flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>221</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Power Low Warning flag mask</td><td>1-bit field to mask lane n Tx Power Low Warning flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>222</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Bias High Alarm flag mask</td><td>1-bit field to mask lane n Tx Bias High Alarm flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>223</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Bias Low Alarm flag mask</td><td>1-bit field to mask lane n Tx Bias Low Alarm flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>224</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Bias High Warning flag mask</td><td>1-bit field to mask lane n Tx Bias High Warning flag. One bit for one lane. Lane order 8, 7,…,1.</td></tr>
<tr><td>225</td><td>1</td><td>RW</td><td>7~0</td><td>M-Tx n Bias Low Warning flag mask</td><td>1-bit field to mask lane n Tx Bias Low Warning flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>226</td><td>1</td><td>RW</td><td>7~0</td><td>M-Rx n LOS flag mask</td><td>1-bit field to mask lane n Rx LOS flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
<tr><td>227</td><td>1</td><td>RW</td><td>7~0</td><td>M-Rx n LOL flag mask</td><td>1-bit field to mask lane n Rx LOL flag. One bit for one lane. Lane order 8,7,…,1.</td></tr>
</table>

Upper Page 10h (whole page is part of Module Control Register Set)						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
228	1	RW	7~0	M-Rx n Power High Alarm flag mask	1-bit field to mask lane n Rx Power High flag. One bit for one lane. Lane order 8,7,…,1.	
229	1	RW	7~0	M-Rx n Power Low Alarm flag mask	1-bit field to mask lane n Rx Power Low Alarm flag. One bit for one lane. Lane order 8,7,…,1.	
230	1	RW	7~0	M-Rx n Power High Warning flag mask	1-bit field to mask lane n Rx Power High Warning flag. One bit for one lane. Lane order 8,7,…,1.	
231	1	RW	7~0	M-Rx n Power Low Warning flag mask	1-bit field to mask lane n Rx Power Low Warning flag. One bit for one lane. Lane order 8,7,…,1.	
232~239	8	RO	7~0	Reserved	No change	
240~255	16	RW	7~0	Custom	No change	

5.3.8 Upper Page 11h (17) Lane Control Registers

Table 29 U11h (17) Lane Control Registers

Upper Page 11h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
~~128~131~~	~~4~~	~~RO~~	7~0	~~Datapath State indicators~~ Reserved	Not needed for ACMIS	
132	1	RO	7~0	Host Lane n Powered up Status	Indicator if a host lane is powered up and SI ready for service. Bits 7 to 0 correspond to host lane 8 to 1.	
133	1	RO	7~0	Media Lane n Power up Status	Indicator if a media lane is powered up and SI ready for service. Bits 7 to 0 correspond to media lane 8 to 1.	
~~134~~	~~1~~	~~RO~~	7~0	~~L-Lane n Data Path State Change flag~~ Reserved.	~~Latched Data Path State Changed flag for lane n, n = 1, …, 8~~. Not needed for ACMIS	
135	1	RO	7~0	L-Tx Lane n Fault flag	Latched Tx Lane n Fault flag, bit field for each lane, n = 8~1.	
136	1	RO	7~0	L-Tx Lane n LOS flag	Latched Tx LOS flag, Bits 0~7 corresponding to media lanes 8~1.	
137	1	RO	7~0	L-Tx n CODR LOL flag	Latched Tx CDR LOL flag, Bits 7~0 corresponding to media lanes 8~1.	
138	1	RO	7~0	L-Tx Adaptive Input Eq. Fault Lane n flag	Latched Tx Adaptive Input Eq. Fault Lane N flag.	
139	1	RO	7~0	L-Tx n Power High Alarm	Latched Tx Power High alarm, bits 7~0 corresponding to media lanes 8~1.	
140	1	RO	7~0	L-Tx n Power Low Alarm	Latched Tx Power Low alarm, bits 7~0 corresponding to media lanes 8~1.	
141	1	RO	7~0	L-Tx n Power High warning	Latched Tx Power High Warning, bits 7~0 corresponding to media lanes 8~1.	
142	1	RO	7~0	L-Tx n Power Low Warning	Latched Tx Power Low Warning, bits 7~0 corresponding to media lanes 8~1.	
143	1	RO	7~0	L-Tx n Bias High Alarm	Latched Tx Bias Current High alarm, bits 7~0 corresponding to media lanes 8~1.	
144	1	RO	7~0	L-Tx n Bias Low Alarm	Latched Tx Bias Current Low alarm, bits 7~0 corresponding to media lanes 8~1.	
145	1	RO	7~0	L-Tx n Bias High Warning	Latched Tx Bias Current High Warning, bits 7~0 corresponding to media lanes 8~1.	
146	1	RO	7~0	L-Tx n Bias Low Warning	Latched Tx Bias Current Low Warning, bits 7~0 corresponding to media lanes 8~1.	
147	1	RO	7~0	L-Rx n LOS	Latched Rx LOS flag, Bits 7~0 corresponding to media lanes 8~1.	
148	1	RO	7~0	L-Rx n CDR LOL	Latched Rx CDR LOL flag, Bits 7~0 corresponding to media lanes 8~1.	
149	1	RO	7~0	L-Rx n Power High Alarm	Latched Rx input Power High alarm, bits 7~0 corresponding to media lanes 8~1.	
150	1	RO	7~0	L-Rx n Power Low Alarm	Latched Rx input Power Low alarm, bits 7~0 corresponding to media lanes 8~1.	
151	1	RO	7~0	L-Rx n Power High warning	Latched Rx input Power High Warning, bits 7~0 corresponding to media lanes 8~1.	
152	1	RO	7~0	L-Rx n Power Low Warning	Latched Rx input Power Low Warning, bits 7~0 corresponding to media lanes 8~1.	

Upper Page 11h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	
153	1	RO	7~0	Reserved		
Lane-Specific Monitors						
154~169	16	RO	7~0	Tx Media Lane n Power	Internally measured Tx output optical power, 16-bit unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). MSB and LSB of the unsigned integer use big endian format with MSB occupies smaller byte address. n = 1, …, 8.	
170~185	16	RO	7~0	Tx Media Lane n Bias Current	Internally measured Tx bias current monitor: 16-bit unsigned integer in 2 uA increments, times the multiplier from U01h.160. MSB and LSB of the unsigned integer use big endian format with MSB occupies smaller byte address. n = 1, …, 8.	
186~201	16	RO	7~0	Rx Media Lane n Power	Internally measured Rx input optical power: unsigned integer in 0.1 uW increments, yielding a total measurement range of 0 to 6.5535 mW (~-40 to +8.2 dBm). MSB and LSB of the unsigned integer use big endian format with MSB occupies smaller byte address. n = 1, …, 8.	
Configuration Error Code Registers (Not required in ACMIS)						
~~202~205~~	~~4~~	~~RO~~	7~0	~~Lane n Config Error Code~~	~~Not required in ACMIS. Use write flow control message instead.~~	
Indicators for Active Control Set, Application Selected (Not required in ACMIS)						
~~206~213~~	~~8~~	~~RO~~	7~0	~~Active Set Lane n Application Code~~	~~ApSel code from Table 24 or Table 45 for lanes 1 to 8. Not required in ACMIS, use Lane Maps instead.~~	
Indicators for Active Control Set, Tx/Rx Controls (Not required in ACMIS)						
~~214~234~~	~~21~~	~~RO~~	7~0	~~Active Set Tx/RX Controls~~	~~Under evaluation of use - editor~~	
235~239	5	RO	7~0	Reserved		
240~255	16	RO	7~0	~~Module TX/RX Media Lane N Wavelength and Fiber Mapping~~ Reserved	~~Suggest moving to U01.~~ Shall be on reserve.	

5.3.9 Upper Page 1Ch (28) Diagnostics – BERT (PRBS) Controls and Counters

Table 30 U1Ch (28) Diagnostics – BERT (PRBS) Controls and Counters

Upper Page 12h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	*Init. Value*
Module PRBS Configuration						
128	1			PRBS Configuration	Contains various PRBS configuration bits, applies to both host and media sides.	
		RW	7	Counter Control	1-bit filed controls the reset behavior of PRBS internal counter. Upon reading PRBS counters listed below, hardware PRBS counters may be cleared or continue to accumulate. 0: Internal data bit and error bit counters reset to zero on read, 1: Internal data bit and error bit counters keeps accumulating on read.	0
		RO	6~0	Reserved		
129	1	RO		Reserved		
Host Side PRBS Controls (for Rx Output and Tx Input)						
130	1	RW	7~0	Host Lane Rx Output PRBS Generator Enable	Bits 7~0 correspond to Rx Output lanes 8 to 1. Per lane, 0: RX Output lane PRBS Generator disable, 1: Rx Output lane PRBS Generator enable.	0
131	1	RW	7~0	Host Lane Tx Input PRBS Checker Enable	Bits 7~0 correspond to Tx Input lanes 8 to 1. Per lane, 0: Tx Input lane PRBS Checker disable, 1: Tx Input lane PRBS Checker enable.	0

Upper Page 12h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	*Init. Value*
132	1	RW	7~0	Host Lane Near End Loopback Control	Per bit per lane. 0: Near end loopback disable, 1: Near end loopback enable.	0
133	1	RW	7~0	Host Lane Far End Loop-back control	Per bit per lane. 0: Far end Loopback disable, 1: Far end Loopback enable.	0
134	1	RW		Host Lane PRBS Clock Source and Pattern Control	Two 4-bit fields select PRBS patterns for both generators and checkers for all lanes	0
			7	Host Lane PRBS Generator Clock Source Select	0: Recovered from input data, 1: Internally generated.	0
			6~4	Recovered Host Lane PRBS Generator Clock Source Lane Select	3-bit field to assign a source lane n, n = 1, …, 8. 0 = Lane 1, …, 7 = Lane 8.	0
			3~0	Host Lane PRBS ~~Generator~~ Pattern Select	0000b: 2^7, 0001b: 2^9, 0010b: 2^15, 0011b: 2^31Q for PAM4, 0100b: 2^23, 0101b: 2^13Q for PAM4, 0110b: 2^31, 0111b: Square wave for PAM4, 1000b~1111b, reserved.	0
135	1	RW	7~0	Host Lane PRBS data and error bit counters freeze	All lane control of freezing the update for data and bit error counters. Note this control takes a snapshot of internal counters for host to read. It does not affect the internal counters. 0: Resume updating 1: Stop updating	
136~137	2			Reserved		
Media Side PRBS Controls						
138	1	RW	7~0	Media Lane Tx Output PRBS Generator Enable	Bits 7~0 correspond to Rx Output lanes 8 to 1. Per lane, 0: Tx Output lane PRBS Generator disable, 1: Tx Output lane PRBS Generator enable.	0
139	1	RW	7~0	Media Lane Rx Input PRBS Checker Enable	Bits 7~0 correspond to Tx Input lanes 8 to 1. Per lane, 0: Rx Input lane PRBS Checker disable, 1: Rx Input lane PRBS Checker enable.	0
140	1	RW	7~0	Media Lane Near End Loopback Control	Bits 7~0 controls lanes 8 to 1 correspondingly. Per lane, 0: Near end loopback disable, 1: Near end loopback enable.	0
141	1	RW	7~0	Media Lane Far End Loop-back control	Bits 7~0 controls lanes 8 to 1 correspondingly. Per lane, 0: Far end Loopback disable, 1: Far end Loopback enable.	0
142	1	RW		Media Lane PRBS Clock Source and Pattern Control		0
			7	Media Lane PRBS Generator Clock Source Select	0: Recovered from input data, 1: Internally generated.	0
			6~4	Recovered Media Lane PRBS Generator Clock Source Lane Select	3-bit field assigns a source lane n, n = 1, …, 8. 0 = Lane 1, …, 7 = Lane 8.	0
			3~0	Media Lane PRBS Generator Pattern Select	0000b: 2^7, 0001b: 2^9, 0010b: 2^15, 0011b: 2^31Q for PAM4, 0100b: 2^23, 0101b: 2^13Q for PAM4, 0110b: 2^31, 0111b: Square wave for PAM4, 1000b~1111b, reserved.	0
143	1	RW	7~0	Media Lane PRBS data and error bit counters freeze	All lane control of freezing the update for data and bit error counters. Note this control takes a snapshot of internal counters for host to read. It does not affect the internal counters. 0: Resume updating 1: Stop updating	

Upper Page 12h						
Byte	*Size*	*Access*	*Bit*	*Byte or Bit Field Name*	*Description*	*Init. Value*
144~145	2	RO	7~0	Reserved		0
Host Lane Data and Error Bit Counters						
146~161	16	RO		Host Side PRBS Data Bit Counters	2-byte 16-bit counter for PRBS data bit counting, with byte order in big endian, that is, smaller address has MSB. Total 16 bytes for 8 lanes and starting from lane 1. This counter receives updates from internal PRBS data bit counts. It starts updating if it is not in freeze and stops updating if in freeze. It uses an ad-hoc floating-point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	0
			15~10	Exponent of Data Bit Counter	6-bit unsigned integer for data bit counter exponent.	0
			9~0	Mantissa of Data Bit Counter	10-bit unsigned integer for data bit counter mantissa.	0
162~177	16	RO		Host Side PRBS Error Bit Counter for Lane n	2-byte 16-bit counter for PRBS error bit counting, with byte order in big endian, that is, smaller address has MSB. Total 16 bytes for 8 lanes and starting from lane 1. This counter receives updates from internal PRBS data bit counts. It starts updating if it is not in freeze and stops updating if in freeze. It uses an ad-hoc floating-point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	0
			15~10	Exponent of Data Bit Counter	6-bit unsigned integer for error bit counter exponent.	0
			9~0	Mantissa of Data Bit Counter	10-bit unsigned integer for error bit counter mantissa.	0
178~179	2			Reserved		
Media Side PRBS Counters						
181~195	16	RO		Media Side PRBS Data Bit Counters	2-byte 16-bit counter for PRBS data bit counting, with byte order in big endian, that is, smaller address has MSB. Total 16 bytes for 8 lanes and starting from lane 1. This counter receives updates from internal PRBS error bit counts. It starts updating if it is not in freeze and stops updating if in freeze. It uses an ad-hoc floating-point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	0
			15~10	Exponent of Data Bit Counter	6-bit unsigned integer for data bit counter exponent.	0
			9~0	Mantissa of Data Bit Counter	10-bit unsigned integer for data bit counter mantissa.	0
196~211	16	RO	7~0	Media Side PRBS Error Bit Counters	2-byte 16-bit counter for PRBS error bit counting, with byte order in big endian, that is, smaller address has MSB. Total 16 bytes for 8 lanes and starting from lane 1. This counter receives updates from internal PRBS error bit counts. It starts updating if it is not in freeze and stops updating if in freeze. It uses an ad-hoc floating-point number format with a 6-bit unsigned exponent and a 10-bit unsigned mantissa.	0
			15~10	Exponent of Error Bit Counter	6-bit unsigned integer for error bit counter exponent.	0
			9~0	Mantissa of Error Bit Counter	10-bit unsigned integer for error bit counter mantissa.	0
212~255	44	RO		Reserved		0

6 APPENDEX

6.1 Appendix A Module PMD Implementations

Each code, for DSFP module, represents a realization of DSFP module based on reach spec and lane topology. Table 31: DSFP Lane Map Code Lookup Table includes all PMD Types in DSFP Spec (Rev. 1.0) and associated Lane Maps. In this table, if there is a multiplexer to mux host lanes 1 and 2 into media lane 1, the host lane 1 and media lane 1 are leading lanes, such as the case of PDM Type 5, 2:1 Mux and 50GAUI-2:50GBASE-SR. While host lane 2 is a trailing lane represented by a sign of "<". The sign "-" below host lane 2 represents the merge of this lane into media lane 1. Note sign ">" can also be used to indicate a training lane in reverse direction.

Similarly, Table 33: 8-Lane Module Lane Map Code Lookup Table includes all PMD Types in OSFP Spec (Rev. 1.93) and associated Lane Maps. For example, Module PMD Type 4 is a 400GBASE-DR4 parallel SMF module. Leading host lanes are 1, 3, 5, and 7 while 2, 4, 6, and 8 are trailing lanes indicated by "<". The same notation applies to wavelength and fiber mapping. An important concept that shall be indicated is the "Minimum Application Configuration". While a 400GAUI-8 DR4 module, as single data link, requires all 8 host lanes and all 4 media lanes as an Application, in a breakout application, it can be configured as 4x100GAUI-2 DR Applications with two host lanes and one media lane connected by a 2:1 multiplexer. This 2:1 combination forms the minimum configuration of an Application for a particular module architecture such as DR4. Obviously an SR8 module has its minimum Application configuration of one host lane and one media lane.

Table 32: 4-Lane Module Lane Map Code Lookup Table is reserved for 4-lane modules for such purpose and shall be populated in future version of this document.

Table 31: DSFP Lane Map Code Lookup Table

PMD TYPE AND LANE MAP CODE	DSFP HW SPEC		LANE MAP						
	MODULE PMD TYPE DESCRIPTION	REFER TO	MIN. APP. CONFIG. HOST+MEDIA	LANE	TOTAL LANE COUNT	TX SIDE LANE NUMBER		RX SIDE LANE NUMBER	
				HOST	**4**	**1**	**2**	**1**	**2**
0	No Application Assigned	NA	NA	-	-	-	-	-	-
1	CR	NA	NA	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Twisted pair	4	1	2	1	2
2	AOC	NA	NA	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Fiber	4	1	2	1	2
3	Parallel Fiber: 100GBASE-SR2	Sec. 3.2 Figure 1	1+1	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Fiber	4	1	2	1	2
4	Dual Port: 10/25/50GBASE-SR	3.1	1+1	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Fiber	4	1	2	1	2

PMD TYPE AND LANE MAP CODE	DSFP HW SPEC		LANE MAP							
	MODULE PMD TYPE DESCRIPTION	REFER TO	MIN. APP. CONFIG. HOST+MEDIA	LANE	TOTAL LANE COUNT	TX SIDE LANE NUMBER		RX SIDE LANE NUMBER	
				HOST	**4**	**1**	**2**	**1**	**2**
5	2:1 Mux and 50GAUI-2: 50GBASE-SR	3.3	2+1	Media	2	1	<	1	<
				Wavelength	1	1	-	1	-
				Fiber	2	1	-	2	-
6	2:1 Mux & 100GAUI-2: 100GBASE-DR	3.4	2+1	Media	1	1	<	1	<
				Wavelength	1	1	-	1	-
				Fiber	2	1	-	2	-
7	Dual Port: 50GBASE-FR	3.1	1+1	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Fiber	4	1	2	1	2
8	2:1 Mux and 50GAUI-2: 50GBASE-FR	3.3	2+1	Media	2	1	<	2	<
				Wavelength	1	1	-	1	-
				Fiber	2	1	-	2	-
9	Dual Port: 50GBASE-LR	3.1	1+1	Media	4	1	2	1	2
				Wavelength	1	1	1	1	1
				Fiber	4	1	2	1	2
10	2:1 Mux and 50GAUI-2: 50GBASE-LR	3.3	2+1	Media	2	1	<	1	<
				Wavelength	1	1	-	1	-
				Fiber	2	1	-	2	-
11	Dual Port 10G/25G/50G-PAM4 Bi-Di	3.5	1+1	Media	4	1	2	1	2
				Wavelength	2	1	1	2	2
				Fiber	2	1	2	1	2
12~127	Reserved for ER/ZR etc.	-	-						
128~255	Custom	-	-	-	-	-	-	-	-

Table 32: 4-Lane Module Lane Map Code Lookup Table

Place holder		

Table 33: 8-Lane Module Lane Map Code Lookup Table

LANE MAP CODE	OSFP HW SPEC		LANE MAP (RX SIDE SYMMETRY ASSUMED)									
	Module PMD Type Description	Refer to	Min. App. Config. Host+Media	Lane	Total TX Lane Count	TX Side Lane Number (RX side symmetry assumed)						
				Host	**8**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
0	Un-defined	NA	NA	-	-								
1	CR	NA	NA	Media	8	1	2	3	4	5	6	7	8
				Wavelength	-	-	-	-	-	-	-	-	-
				Twisted pair	8	1	2	3	4	5	6	7	8
2	AOC	NA	NA	Media	8	1	2	3	4	5	6	7	8
				Wavelength	1	1	1	1	1	1	1	1	1
				Fiber	8	1	2	3	4	5	6	7	8

3	Parallel Fiber: 400GSR8	Sec. 9.2 Figure 9-2	1+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	1	1	1	1	1	1	1	1	1
				Fiber	8	1	2	3	4	5	6	7	8
4	400GBASE-DR4 Parallel SMF	9.1 Figure 9-1	2+1	Media	4	1	<	2	<	3	<	4	<
				Wavelength	1	1	-	1	-	1	-	1	-
				Fiber	4	1	-	2	-	3	-	4	-
5	400G-FR4 (IC: 8x50G PAM4 to 4x100G PAM4)	Sec. 9.4 Figure 9-4	8+1	Media	4	1	<	2	<	3	<	4	<
				Wavelength	4	1	-	2	-	3	-	4	-
				Fiber	1	1	-	<	-	<	-	<	-
6	400G-FR8 (IC: 1x8x50G PAM4 or 2x4x50G PAM4)	Sec. 9.5 Figure 9-5	8+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	8	1	2	3	4	5	6	7	8
				Fiber	1	1	<	<	<	<	<	<	<
7	2x200G-2xFR4 (IC: 2x4x50G PAM CDR)	Sec.9.6 Figure 9-6	4+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	4	1	2	3	4	1	2	3	4
				Fiber	2x1	1	<	<	<	2	<	<	<
8	2x100G-2xCWDM4 (IC: 2x4x25G NRZ CDR)	Sec. 9.7 Figure 9-7	4+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	4	1	2	3	4	1	2	3	4
				Fiber	2x1	1	<	<	<	2	<	<	<
9	400G-LR8 (IC: 1x8x50G PAM4 or 2x4x50G PAM4)	Sec. 9.5	8+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	8	1	2	3	4	5	6	7	8
				Fiber	1	1	<	<	<	<	<	<	<
10	400G-SR4.2 Bi-Di	Sec. 9.3 Figure 9-3	1+1	Media	8	1	2	3	4	5	6	7	8
				Wavelength	2	1	2	1	2	1	2	1	2
				Fiber	2	1	2	3	4	5	6	7	8
11~127	Reserved for ER/ZR etc.	-	-	Media	-	-	-	-	-	-	-	-	-
				Wavelength	-	-	-	-	-	-	-	-	-
				Fiber	-	-	-	-	-	-	-	-	-
128~ 255	Custom	-	-	-	-	-	-	-	-	-	-	-	-

6.2 Appendix B Host and media lane advertising codes

This section provides the advertising codes for both host electrical and module media interfaces. The codes for applications supported by the module are entered by the module into the Module Host-Media Interfaces advertising registers in L00h.85, also defined in U04h.129 in ACMIS. (Recommend to use U04h.128 - Editor) identifies which of the media interface code tables. The following tables include all items listed in CMIS 3.0 Appendix C. Some legacy CPRI codes have been included per user request but no ID/Code has been assigned at the publication of this draft.

Table 34 (78 in CMIS) Module Host Electrical Interfaces Code

ID	CODE (HEX)	APPLICATION NAME	DATA RATE, GB/S	LANE COUNT	LANE RATE, GBD	MODULA-TION	B/SYM
0	0	Undefined					
Ethernet Applications							
1	1	1000BASE -CX (Clause 39)	1.25	1	1.25	NRZ	1
2	2	XAUI (Clause 47)	12.50	4	3.125	NRZ	1
3	3	XFI (SFF INF-8071i)	9.95-11.18	1	9.95-11.18	NRZ	1
4	4	SFI (SFF-8431)	9.95-11.18	1	9.95-11.18	NRZ	1

5	5	25GAUI C2M (Annex 109B)	25.78	1	25.78125	NRZ	1
6	6	XLAUI C2M (Annex 83B)	41.25	4	10.3125	NRZ	1
7	7	XLPPI (Annex 86A)	41.25	4	10.3125	NRZ	1
8	8	LAUI-2 C2M (Annex 135C)	51.56	2	25.78125	NRZ	1
9	9	50GAUI-2 C2M (Annex 135E)	53.13	2	26.5625	NRZ	1
10	A	50GAUI-1 C2M (Annex 135G)	53.13	1	26.5625	PAM4	2
11	B	CAUI-4 C2M (Annex 83E)	103.13	4	25.78125	NRZ	1
12	C	100GAUI-4 C2M (Annex 135E)	106.25	4	26.5625	NRZ	1
13	D	100GAUI-2 C2M (Annex 135G)	106.25	2	26.5625	PAM4	2
14	E	200GAUI-8 C2M (Annex 120C)	212.50	8	26.5625	NRZ	1
15	F	200GAUI-4 C2M (Annex 120E)	212.50	4	26.5625	PAM4	2
16	10	400GAUI-16 C2M (Annex 120C)	425.00	16	26.5625	NRZ	1
17	11	400GAUI-8 C2M (Annex 120E)	425.00	8	26.5625	PAM4	2
18	12	Reserved					
19	13	10GBASE-CX4 (Clause 54)	12.50	4	3.125	NRZ	1
20	14	25GBASE-CR CA-L (Clause 110)	25.78	1	25.78125	NRZ	1
21	15	25GBASE-CR CA-S (Clause 110)	25.78	1	25.78125	NRZ	1
22	16	25GBASE-CR CA-N (Clause 110)	25.78	1	25.78125	NRZ	1
23	17	40GBASE-CR4 (Clause 85)	41.25	4	10.3125	NRZ	1
24	18	50GBASE-CR (Clause 126)	53.13	1	26.5625	PAM4	2
25	19	100GBASE-CR10 (Clause 85)	103.13	10	10.3125	NRZ	1
26	1A	100GBASE-CR4 (Clause 92)	103.13	4	25.78125	NRZ	1
27	1B	100GBASE-CR2 (Clause 136)	106.25	2	26.5625	PAM4	2
28	1C	200GBASE-CR4 (Clause 136)	212.50	4	26.5625	PAM4	2
29	1D	400G CR8 ()	425.00	8	26.5625	PAM4	2
30	1E	1000BASE -T (Clause 40)	1.12	4	0.125	PAM5	2.236068
31	1F	2.5GBASE-T (Clause 126)	2.50	4	0.200	PAM16	3.125
32	20	5GBASE-T (Clause 126)	5.00	4	0.400	PAM16	3.125
33	21	10GBASE-T (Clause 55)	10.00	4	0.800	PAM16	3.125
34	22	25GBASE-T (Clause 113)	25	4	2.000	PAM16	3.125
35	23	40GBASE-T (Clause 113)	40	4	3.200	PAM16	3.125
36	24	50GBASE-T ()					
Fibre Channel Applications							
37	25	8GFC (FC-PI -4)	8.50	1	8.500	NRZ	1
38	26	10GFC (10GFC)	10.52	1	10.51875	NRZ	1
39	27	16GFC (FC-PI -5)	14.03	1	14.025	NRZ	1
40	28	32GFC (FC-PI -6)	28.05	1	28.050	NRZ	1
41	29	64GFC (FC-PI -7)	57.80	1	28.900	PAM4	2
42	2A	128GFC (FC-PI -6P)	112.20	4	28.050	NRZ	1
43	2B	256GFC (FC-PI -7P)	231.20	4	28.900	PAM4	2
InfiniBand Applications							
44	2C	IB SDR (Arch.Spec.Vol.2 R.1.3.1)	2.5 - 30	1, 2, 4, 8, 12	2.5	NRZ	1
45	2D	IB DDR (Arch.Spec.Vol.2 R.1.3.1)	5.0 - 60	1, 2, 4, 8, 12	5.0	NRZ	1
46	2E	IB QDR (Arch.Spec.Vol.2 R.1.3.1)	10 - 120	1, 2, 4, 8, 12	10.0	NRZ	1
47	2F	IB FDR (Arch.Spec.Vol.2 R.1.3.1)	14 - 169	1, 2, 4, 8, 12	14.0625	NRZ	1
48	30	IB EDR (Arch.Spec.Vol.2 R.1.3.1)	26 - 309	1, 2, 4, 8, 12	25.78125	NRZ	1

49	31	IB HDR (Arch.Spec.Vol.2 R.1.3.1)	52 - 618	1, 2, 4, 8, 12	26.5625	PAM4	2
50	32	IB NDR	Nx100G				
CPRI Applications							
51	33	E.96 (CPRI Specification V7.0)	9.83	1	9.8304	NRZ	1
52	34	E.99 (CPRI Specification V7.0)	10.14	1	10.1376	NRZ	1
53	35	E.119 (CPRI Specification V7.0)	12.17	1	12.16512	NRZ	1
54	36	E.238 (CPRI Specification V7.0)	24.33	1	24.33024	NRZ	1
OTN Applications							
55	37	OTL3.4 (ITU-T G.709/Y.1331 G.Sup58) See XLAUI (overclocked)	43	4	10.7546	NRZ	1
56	38	OTL4.10 (ITU-T G.709/Y.1331 G.Sup58) See CAUI-10 (overclocked)	112	10	11.1810	NRZ	1
57	39	OTL4.4 (ITU-T G.709/Y.1331 G.Sup58)See CEI-28G-VSR	112	4	27.9525	NRZ	1
58	3A	OTLC.4 (ITU-T G.709/Y.1331 G.Sup58) See CEI-28G-VSR	112	4	28.0762	NRZ	1
59	3B	FOIC1.4 (ITU-T G.709/Y.1331 G.Sup58) See CEI-28G-VSR	112	4	27.9524	NRZ	1
60	3C	FOIC1.2 (ITU-T G.709/Y.1331 G.Sup58) See CEI-56G-VSR-PAM4	112	2	27.9524	PAM4	2
61	3D	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	224	8	27.9523	NRZ	1
62	3E	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	224	4	27.9523	PAM4	2
63	3F	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	447	16	27.9523	NRZ	1
64	40	FOIC2.8 (ITU-T G.709/Y.1331 G.Sup58	447	8	27.9523	PAM4	2
61: 191	3D:BF	Reserved					
192:254	C0:FF	Custom					
255	FF	End of List					

1 Table 35 (79 in CMIS)- 850 nm MM media interface advertising codes

ID	CODE (HEX)	APPLICATION NAME	APPLICATION DATA RATE, GB/S	LANE COUNT	LANE DATA RATE, GBD	MODULA-TION	B/SYM
0	0	Undefined					
Ethernet Applications							
1	1	10GBASE-SW (Clause 52)	9.95	1	9.95328	NRZ	1
2	2	10GBASE-SR (Clause 52)	10.31	1	10.3125	NRZ	1
3	3	25GBASE-SR (Clause 112)	25.78	1	25.78125	NRZ	1
4	4	40GBASE-SR4 (Clause 86)	41.25	4	10.3125	NRZ	1
5	5	40GE SWDM4 MSA Spec	41.25	4	10.3125	NRZ	1
6	6	40GE BiDi	41.25	2	20.625	NRZ	1
7	7	50GBASE-SR (Clause 138)	53.13	1	26.5625	PAM4	2
8	8	100GBASE-SR10 (Clause 86)	103.13	10	10.3125	NRZ	1

9	9	100GBASE-SR4 (Clause 95)	103.13	4	25.78125	NRZ	1
10	A	100GE SWDM4 MSA Spec	103.13	4	25.78125	NRZ	1
11	B	100GE BiDi	106.25	2	25.5625	PAM4	2
12	C	100GBASE-SR2 (Clause 138)	106.25	2	26.5625	PAM4	2
13	D	100G-SR					
14	E	200GBASE-SR4 (Clause 138)	212.50	4	26.5625	PAM4	2
15	F	400GBASE-SR16 (Clause 123)	425.00	16	26.5625	NRZ	1
16	10	400G-SR8					
17	11	400G-SR4					
18	12	800G-SR8					
Fibre Channel Applications							
19	13	8GFC-MM (FC-PI -4)	8.50	1	8.500	NRZ	1
20	14	10GFC-MM (10GFC)	10.52	1	10.51875	NRZ	1
21	15	16GFC-MM (FC-PI -5)	14.03	1	14.025	NRZ	1
22	16	32GFC-MM (FC-PI -6)	28.05	1	28.050	NRZ	1
23	17	64GFC-MM (FC-PI -7)	57.80	1	28.900	PAM4	2
24	18	128GFC-MM4 (FC-PI -6P)	112.20	4	28.050	NRZ	1
25	19	256GFC-MM4 (FC-PI -7P)	231.20	4	28.900	PAM4	2
Ethernet Applications							
26	1A	400GE BiDi	425.00	8	26.5625	PAM4	2
27: 191	1A:BF	Reserved					
192:255	C0:FF	Custom					

1 Table 36 (80 in CMIS) SM media interface advertising codes

ID	CODE (HEX)	APPLICATION NAME	APPLICATION DATA RATE, GB/S	LANE COUNT	LANE SIGNAL RATE, GBD	MODULA-TION	B/SYM
0	0	Undefined					
Ethernet Applications							
1	1	10GBASE-LW (Cl 52)	9.95	1	9.953	NRZ	1
2	2	10GBASE-EW (Cl 52)	9.95	1	9.953	NRZ	1
3	3	10G-ZW	9.95	1	9.953	NRZ	1
4	4	10GBASE-LR (Cl 52)	10.31	1	10.3125	NRZ	1
5	5	10GBASE-ER (Cl 52)	10.31	1	10.3125	NRZ	1
6	6	10G-ZR	10.31	1	10.3125	NRZ	1
7	7	25GBASE-LR (Cl 114)	25.78	1	25.78125	NRZ	1
8	8	25GBASE-ER (Cl 114)	25.78	1	25.78125	NRZ	1
9	9	40GBASE-LR4 (Cl 87)	41.25	4	10.3125	NRZ	1
10	A	40GBASE-FR (Cl 89)	41.25	1	41.25	NRZ	1

11	B	50GBASE-FR (Cl 139)	53.13	1	26.5625	PAM4	2
12	C	50GBASE-LR (Cl 139)	53.13	1	26.5625	PAM4	2
13	D	100GBASE-LR4 (Cl 88)	103.13	4	25.78125	NRZ	1
14	E	100GBASE-ER4 (Cl 88)	103.13	4	25.78125	NRZ	1
15	F	100G PSM4 MSA Spec	103.13	4	25.78125	NRZ	1
16	10	100G CWDM4 MSA Spec	103.13	4	25.78125	NRZ	1
17	11	100G 4WDM-10 MSA Spec	103.13	4	25.78125	NRZ	1
18	12	100G 4WDM-20 MSA Spec	103.13	4	25.78125	NRZ	1
19	13	100G 4WDM-40 MSA Spec	103.13	4	25.78125	NRZ	1
20	14	100GBASE-DR (Cl 140)	106.25	1	53.125	PAM4	2
21	15	100G-FR					
22	16	100G-LR					
23	17	200GBASE-DR4 (Cl 121)	212.50	4	26.5625	PAM4	2
24	18	200GBASE-FR4 (Cl 122)	212.50	4	26.5625	PAM4	2
25	19	200GBASE-LR4 (Cl 122)	212.50	4	26.5625	PAM4	2
26	1A	400GBASE-FR8 (Cl 122)	425.00	8	26.5625	PAM4	2
27	1B	400GBASE-LR8 (Cl 122)	425.00	8	26.5625	PAM4	2
28	1C	400GBASE-DR4 (Cl 124)	425.00	4	53.125	PAM4	2
29	1D	400G-FR4					
30	1E	400G-LR4					
Fibre Channel Applications							
31	1F	8GFC-SM (FC-PI -4)	8.50	1	8.500	NRZ	1
32	20	10GFC-SM (10GFC)	10.52	1	10.51875	NRZ	1
33	21	16GFC-SM (FC-PI-5)	14.03	1	14.025	NRZ	1
34	22	32GFC-SM (FC-PI-6)	28.05	1	28.050	NRZ	1
35	23	64GFC-SM (FC-PI-7)	57.80	1	28.900	PAM4	2
36	24	128GFC-PSM4 (FC-PI-6P)	112.20	4	28.050	NRZ	1
37	25	256GFC-PSM4 (FC-PI-7P)	231.20	4	28.900	PAM4	2
38	26	128GFC-CWDM4 (FC-PI-6P)	112.20	4	28.050	NRZ	1
39	27	256GFC-CWDM4 (FC-PI-7P)	231.20	4	28.900	PAM4	2
40-43	28-2B	Reserved					
OTN Applications							
44	2C	4I1-9D1F	112	4	28	NRZ	1
45	2D	4L1-9C1F	112	4	28	NRZ	1
46	2E	4L1-9D1F	112	4	28	NRZ	1

47	2F	C4S1-9D1F	112	4	28	NRZ	1
48	30	C4S1-4D1F	224	4	27.9523	PAM4	2
49	31	4I1-4D1F	224	4	27.9523	PAM4	2
50	32	8R1-4D1F	447	8	27.9523	PAM4	2
51	33	8I1-4D1F	447	8	27.9523	PAM4	2
52:55	34:37	Reserved					
CPRI Applications							
56	38	10G-SR	9.8304	1	9.8304	NRZ	1
57	39	10G-LR	9.8304	1	9.8304	NRZ	1
58	3A	25G-SR	24.33024	1	24.33024	NRZ	1
59	3B	25G-LR	24.33024	1	24.33024	NRZ	1
60	3C	10G-LR-BiDi	9.8304	1	9.8304	NRZ	1
61	3D	25G-LR-BiDi	24.33024	1	24.33024	NRZ	1
62: 191	3E:BF	Reserved					
192:255	C0:FF	Custom					

Table 37 (81 in CMIS) Passive Copper Cable interface advertising codes

ID	CODE (HEX)	APPLICATION NAME
0	0	Undefined
1	1	Copper cable, see Page 00h Bytes 202 - 208 for description
2:191	2:BF	Reserved
192:255	C0:FF	Custom

Note: Details for the cable assembly interface are defined using the host electrical codes in Table 34 (78 in CMIS) Module Host Electrical Interfaces Code.

Table 38 (Table 82 in CMIS) Active Cable assembly media interface advertising codes

ID	CODE (HEX)	APPLICATION NAME
0	0	Undefined
1	1	Active Cable assembly with BER < 10^-12
2	2	Active Cable assembly with BER < 5x10^-5
3	3	Active Cable assembly with BER < 2.4x10^-4
4:191	4:BF	Reserved
192:255	C0:FF	Custom

Note: Details for the cable assembly interface are defined using the host electrical codes in Table 34 (78 in CMIS) Module Host Electrical Interfaces Code.

Table 39 (Table 83 in CMIS) Base-T media interface advertising codes

ID	CODE (HEX)	APPLICATION NAME	APPLICATION DATA RATE, GB/S	LANE COUNT	LANE SIGNAL RATE, GBD	MODULATION	
0	0	Undefined					
Ethernet Applications							
1	1	1000BASE -T (Clause 40)	1.12	4	0.125	PAM5	2.236068
2	2	2.5GBASE-T (Clause 126)	2.50	4	0.200	PAM16	3.125
3	3	5GBASE-T (Clause 126)	5.00	4	0.400	PAM16	3.125
4	4	10GBASE-T (Clause 55)	10.00	4	0.800	PAM16	3.125
5:191	5:BF	Reserved					
192:255	C0:FF	Custom					

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